

Application of Polycrystalline SiGe for Gain Control in SiGe Heterojunction Bipolar Transistors

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Motivation

- High f_{\max} in SiGe HBT's requires high Ge concentration in the base & high collector doping to minimise delay times
- High Ge content & narrow base gives high gain β
- High collector doping gives low breakdown voltage BV_{CEO}

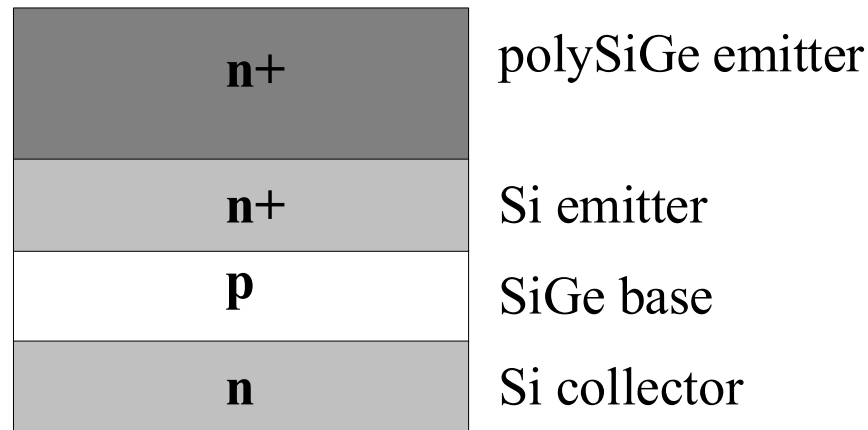
$$BV_{\text{CEO}} = \frac{BV_{\text{CBO}}}{\sqrt[n]{\beta}}$$

\Rightarrow Method is needed to reduce the gain without modifying the base Ge and B profiles



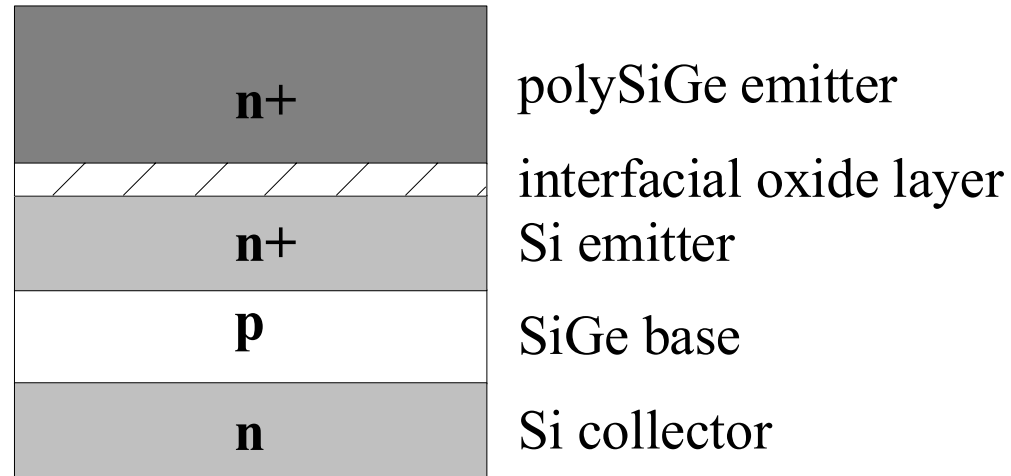
Concept

- Base current control (gain) by incorporating Ge into the polysilicon emitter
- This method allows gain control independently of the Ge and B profiles in the base



Concept

Interfacial layer between polySiGe layer and Si emitter

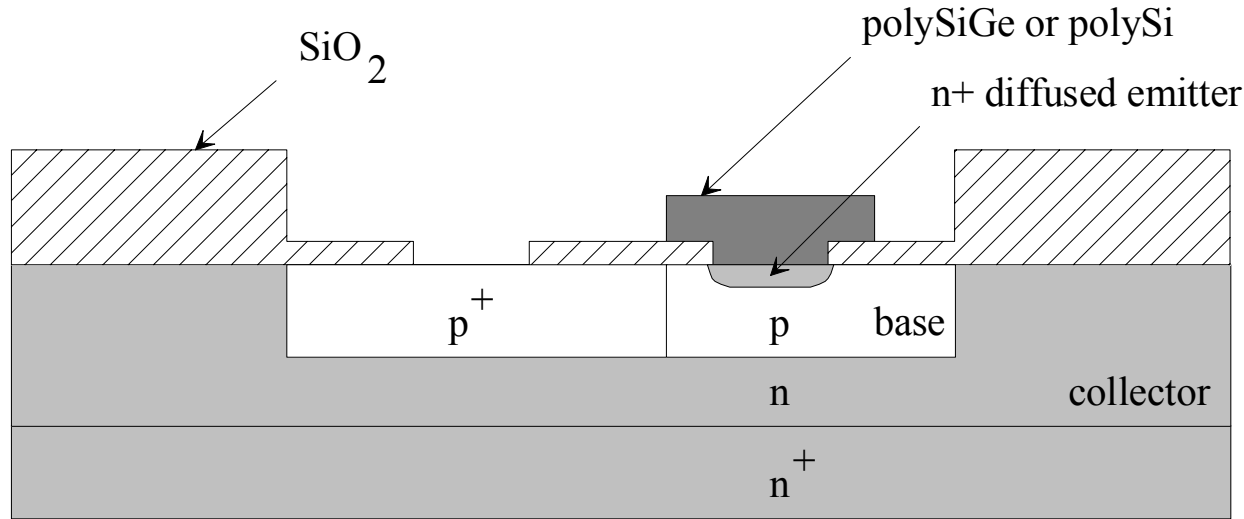


- PolySiGe emitter increases base current
 \Rightarrow reduces β
- Interfacial oxide layer reduces base current
 \Rightarrow increases β



Transistor fabrication

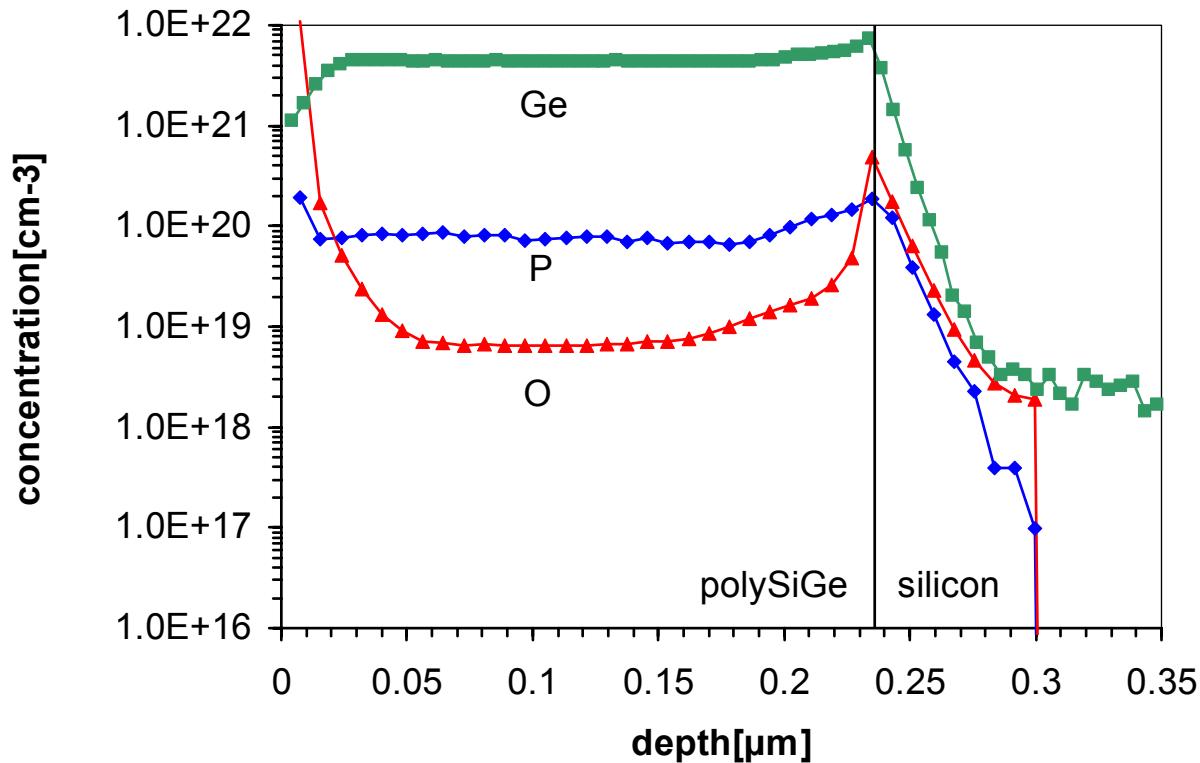
Silicon bipolar transistors were fabricated with in-situ doped polySiGe emitters with Ge contents 0 to 33%



- Ex-situ HF etch to clean surface and remove native oxide
- PolySiGe layer was deposited in Thermo VG Semicon CV200 LPCVD system at 540°C
- PolySiGe emitter was completed by annealing for 30s at either 900 or 800°C



Experimental results

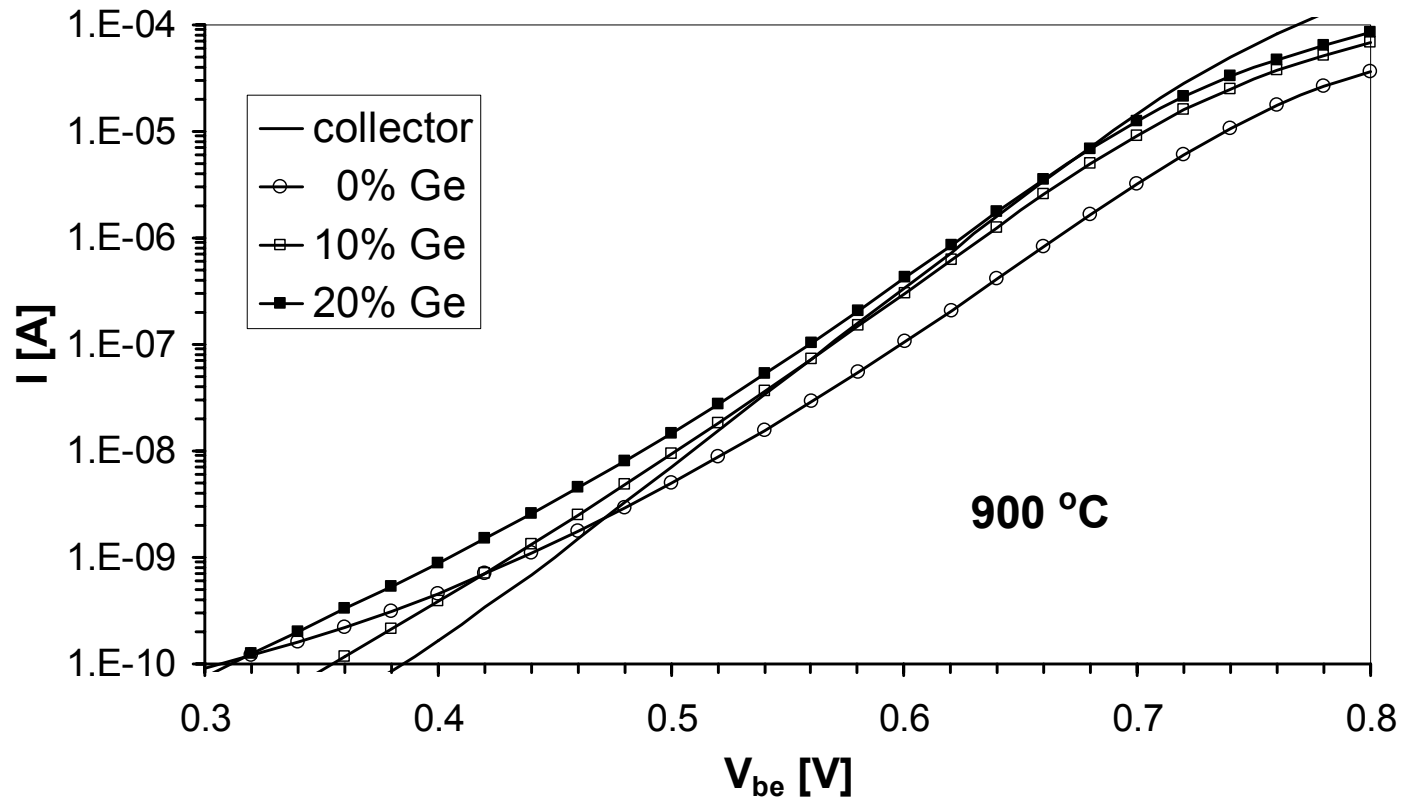


SIMS profile for a polySi_{0.89}Ge_{0.11} emitter annealed for 30s at 800°C

Ge in polySiGe region	4.5e21cm-3
Oxygen dose	6.4e14cm-2
Oxide thickness	0.21nm



Experimental results

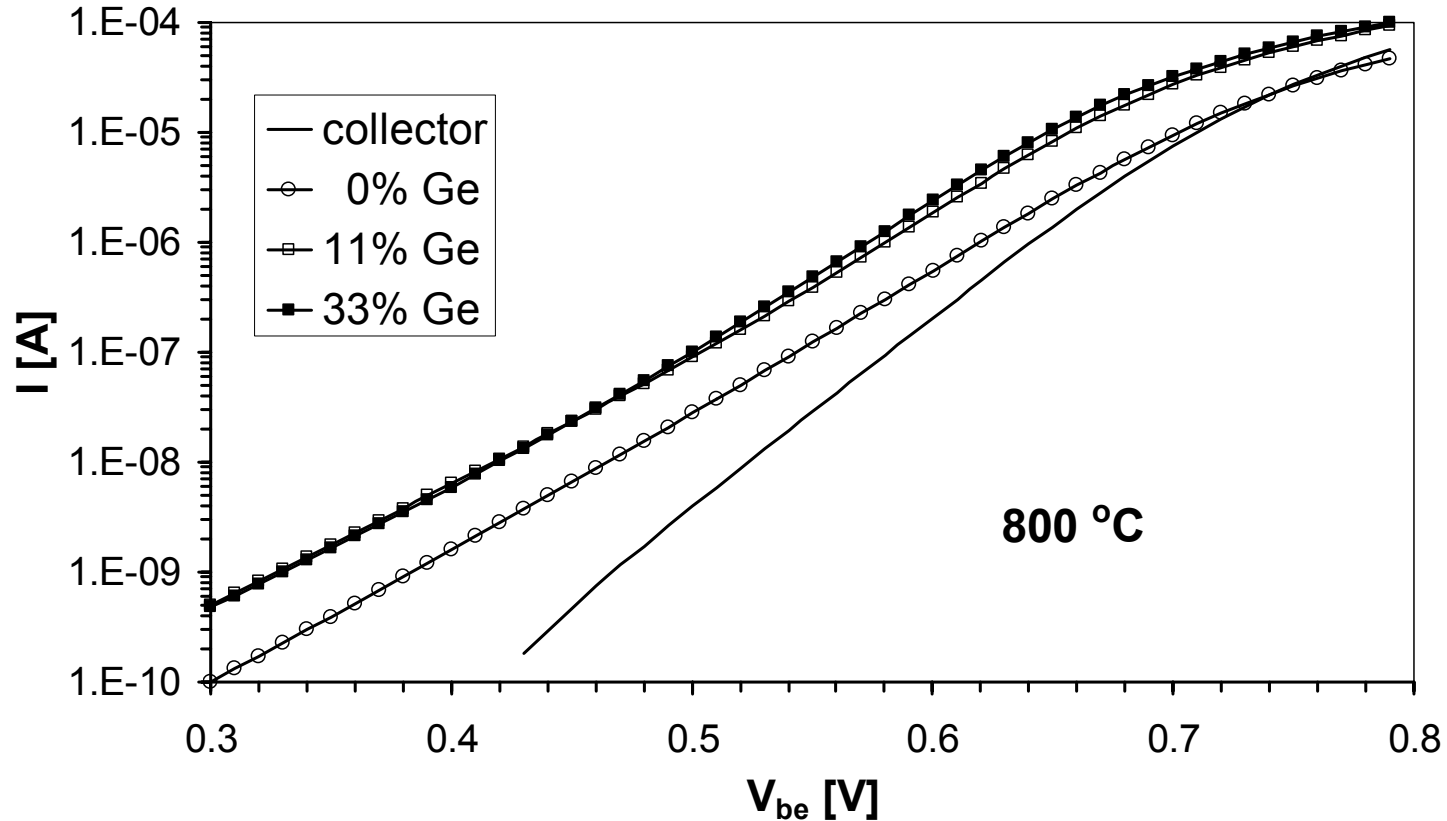


900 °C	0% Ge	10% Ge	19% Ge
Ideality factors ($V_{BE}=0.6V$)	1.2	1.14	1.13
Increase in I_B		2.9	4

=> Increasing Ge causes I_B to increase



Experimental results

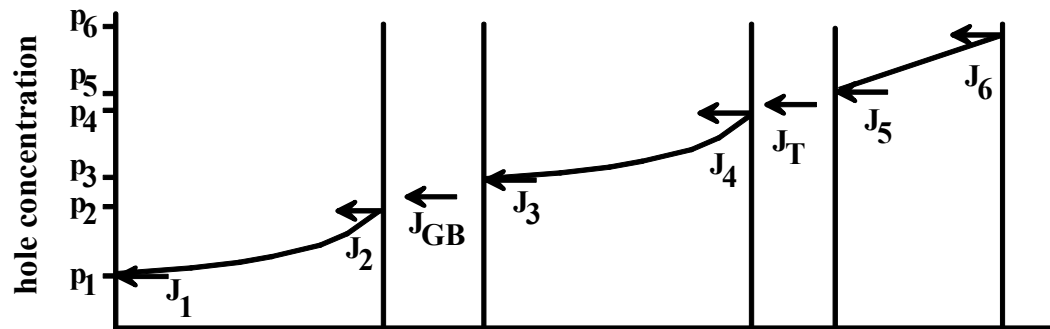
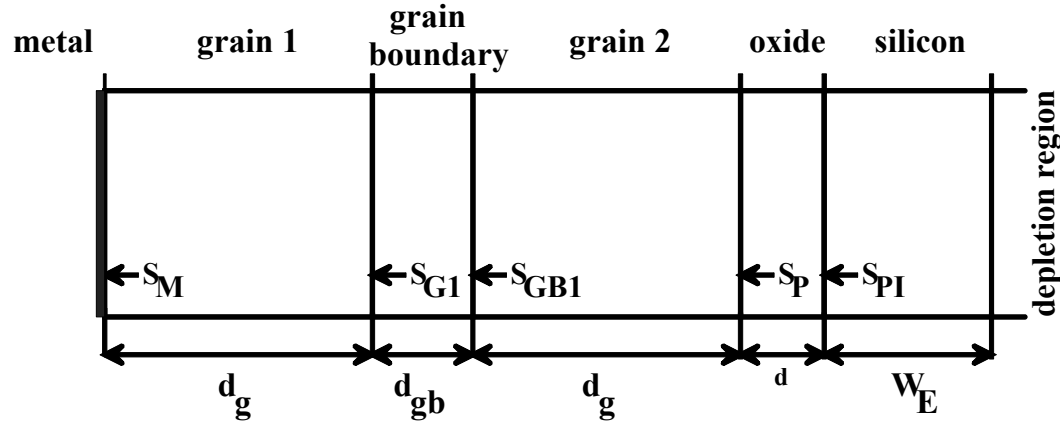


800 °C	0% Ge	11% Ge	33% Ge
Ideality factors ($V_{BE}=0.55V$)	1.3	1.3	1.2
Increase in I_B		3.3	4

\Rightarrow Again, Ge causes I_B to increase



Theory



$$J_1 = qS_M p_{1SiGe}$$

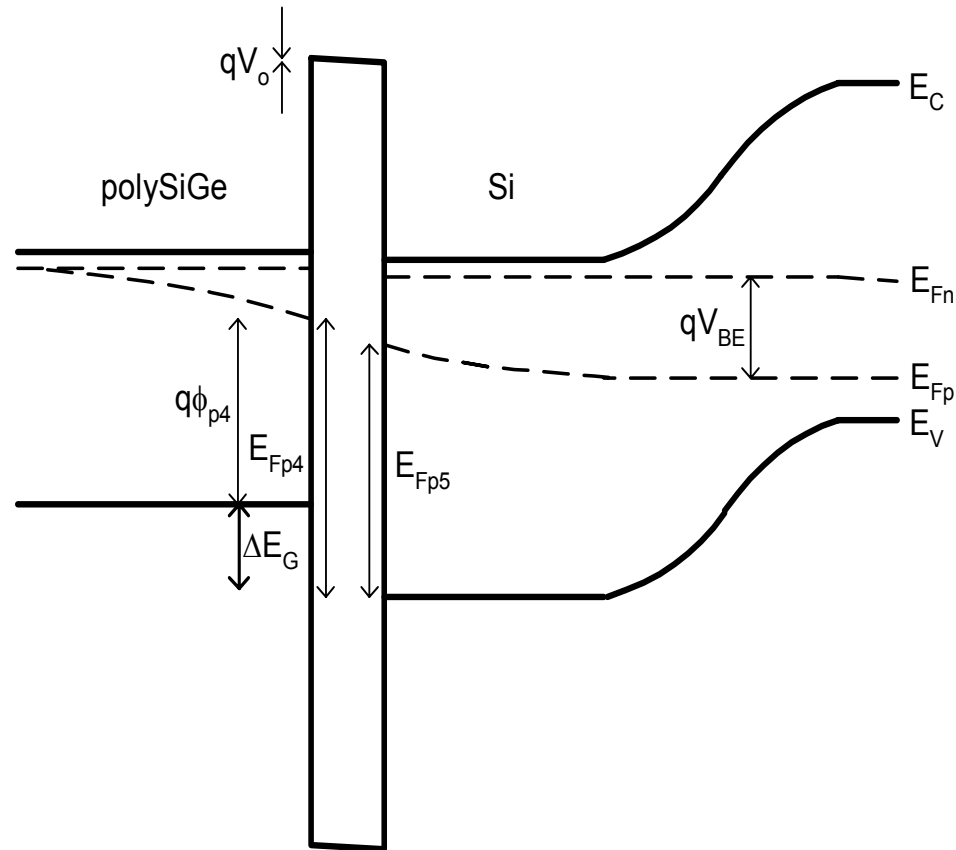
$$J_4 = qS_P p_{4SiGe}$$

$$S_P = a_g - \frac{b_g^2}{a_g + S_{GB1}}$$

where a_g and b_g are depending on the physical properties of the grain (D_{pSiGe} , L_{pSiGe} and d_g)



Theory



- Transport of charge carriers by tunneling through interfacial oxide
- Quasi Fermi level E_{FP4} contains the bandgap difference



Theory

Effective recombination velocity at the right side of the oxide layer:

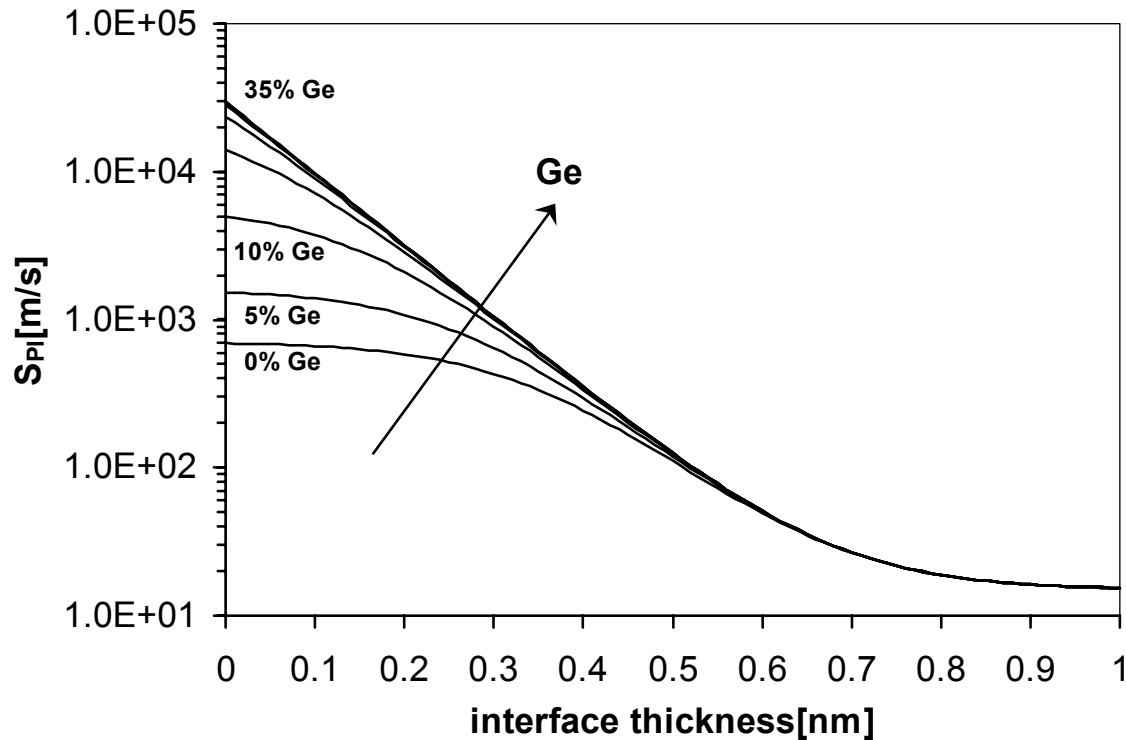
$$S_{PI} = S_I + \left(\frac{T_I(S_P + S_I)}{\frac{T_I}{F} + S_P + S_I} \right)$$

where T_I models the tunneling through the interfacial oxide,
F represents the effects of the Ge:

$$F = \frac{N_{VSiGe}}{N_{VSi}} \exp\left(\frac{\Delta E_G}{kT}\right)$$



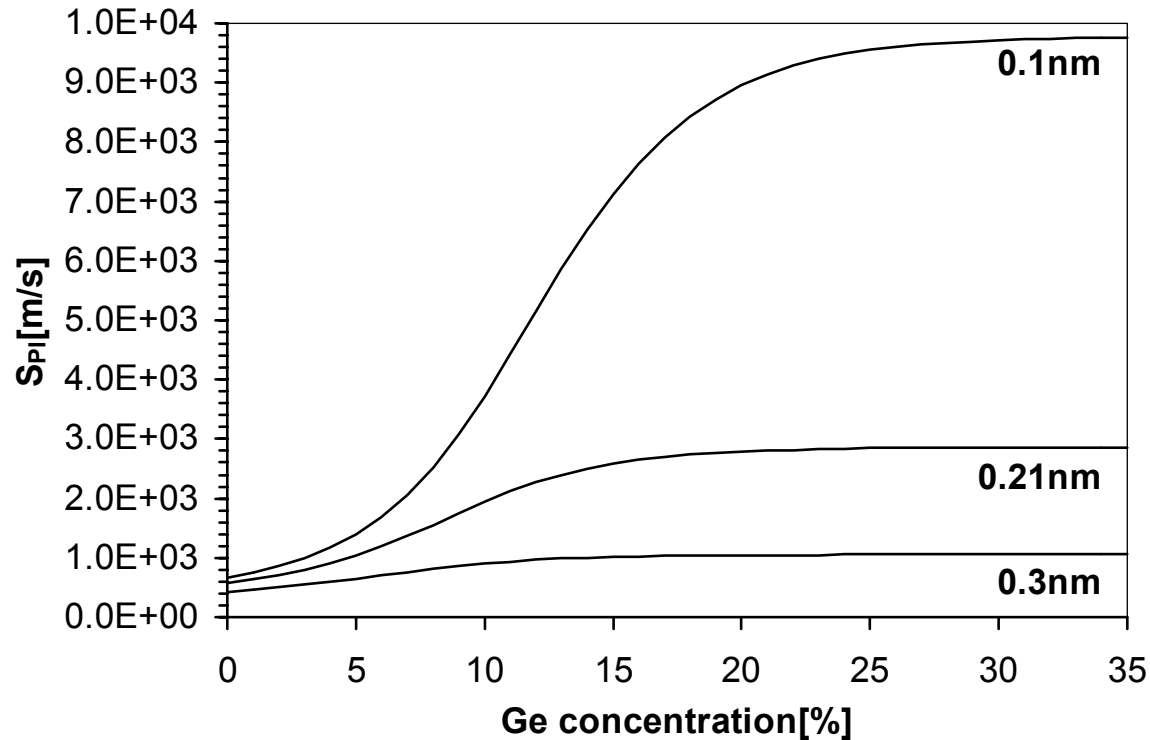
Theory



- For low interfacial thickness T_I is large $\Rightarrow S_{PI} \approx F S_P$
- For high interfacial thickness $S_{PI} \Rightarrow S_{PI} \approx S_I$
- Increase 0% \Rightarrow 10% Ge increases S_{PI} by 3.4
- Increase 0% \Rightarrow 19% Ge increases S_{PI} by 4.8



Theory



- Ge saturates for concentrations $> 20\%$
- Little benefit to increase Ge content over 20%



Comparison of theoretical & experimental results

	800°C			900°C		
Ge concentration [%]	0	11	33	0	10	19
Increase in I_B (experimental)		3.3	4		2.9	4
Increase in I_B (theoretical)		3.4	4.8		3.4	4.8

=> good agreement between theory and experiment



Conclusions

- Incorporation of Ge into a polySi emitter allows the base current to be adjusted independently of the base profile
- Measured results show that Ge content of:
 - 10% gives an increase in base current by a factor of 2.9
 - 19% gives an increase in base current by a factor of 4.0
- Good agreement between theory and experiment
- Theory predicts that Ge saturates for concentrations $> 20\%$
- Theory predicts that higher factors could be achieved by reducing the interfacial layer thickness.

