SiGe pMOSFETs Fabricated on Novel SiGe Virtual Substrates Grown on 10µm x 10 µm Pillars

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Summary

• pMOSFETs fabricated on limited area growth SiGe virtual substrates
• SiGe virtual substrate fabrication
  • Limited area reduces cross hatch on the wafer surface
• Device fabrication
• Electrical results
  • Improved performance of SiGe over Si devices
• Conclusion
Limited Area Growth

• Epitaxial growth zone constrained
  • Growth occurs in small localised areas on the wafer
  • Not across the whole of the wafer.

• Virtual substrate grown on 10µm x 10µm silicon pillars
  • Growth zone constrained by pillars

• MOSFETs fabricated on virtual substrates on top of these pillars
Virtual Substrate Fabrication

- SiGe virtual substrate grown on silicon pillars

![Diagram showing SiGe virtual substrate growth on silicon pillars with specified dimensions.](image-url)
Virtual Substrate Formation

• SiGe lattice constant different to Si
  • Si – 5.43Å
  • Ge – 5.66 Å

• Virtual substrate needs to allow for the difference in lattice constant.
  • Linearly graded layer 0% Ge to 30% Ge

• Creation of misfit dislocations
Creation of Misfit Dislocations

SILICON
GERMANIUM

MISFIT
DISLOCATION

SILICON
Misfit Dislocations

MISFIT DISLOCATION

THREADING ARM

SLIPPED REGION

WAFER SURFACE

THREADING ARMS GLIDE IN \(<111>\) PLANE

GLIDING THREADING ARMS INCREASE LENGTH OF MISFIT DISLOCATION

SiGe VIRTUAL SUBSTRATE
Infinite Area

SiGe VIRTUAL SUBSTRATE

SURFACE CROSSHATCH
Limited Area Improvements

• Misfit dislocations can only terminate if:
  • They interact with another dislocation
  • They reach the edge of the wafer
  • They reach the edge of a limited area growth zone

• Interactions between orthogonal misfit dislocations lead to crosshatch

• Limited area allows misfit dislocations to terminate at the edge of the limited area growth zone
  • Reduces number of interactions and therefore amount of crosshatch on the wafer surface
Dislocation Network

INFINITE AREA

LIMITED AREA

Device Processing (1)

- TRENCHES
- PHOS. SUBSTRATE IMPLANTATION + RTP
- MBE SiGe LAYER GROWTH

- SILICON SUBSTRATE
- SILICON PILLAR
Device Processing (2)

LTO FIELD OXIDE

ACTIVE AREA

TRENCH INFILL

MOSFET DEVICE
Device Processing (3)

200nm Insitu Doped Poly Gate Electrode

5nm Gate Oxide

Sidewall Spacer

Source

Drain

HDD : 5e15 45keV BF$_2$

Extension : 1e14 33keV BF$_2$

Anneal : 800C, 30 minutes
Device & Substrate

- SiGe VIRTUAL SUBSTRATE
- MOSFET
- TRENCH
- Si SUBSTRATE
- METAL

2000 nm
## Layer Structure

<table>
<thead>
<tr>
<th>Layer Description</th>
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<tbody>
<tr>
<td>5nm Gate Oxide</td>
</tr>
<tr>
<td>2nm Si Cap</td>
</tr>
<tr>
<td>2nm Si&lt;sub&gt;0.7&lt;/sub&gt;Ge&lt;sub&gt;0.3&lt;/sub&gt; Cap</td>
</tr>
<tr>
<td>5nm Si&lt;sub&gt;0.3&lt;/sub&gt;Ge&lt;sub&gt;0.7&lt;/sub&gt; Channel</td>
</tr>
<tr>
<td>250nm Si&lt;sub&gt;0.7&lt;/sub&gt;Ge&lt;sub&gt;0.3&lt;/sub&gt; Relaxed Buffer Layer</td>
</tr>
<tr>
<td>1µm Si&lt;sub&gt;1&lt;/sub&gt;Ge&lt;sub&gt;0&lt;/sub&gt; to Si&lt;sub&gt;0.7&lt;/sub&gt;Ge&lt;sub&gt;0.3&lt;/sub&gt; Linearly Graded Buffer Layer</td>
</tr>
<tr>
<td>Silicon Substrate</td>
</tr>
</tbody>
</table>
$V_{ds}$ vs $I_{ds}$ 2µm Devices

$V_{gt}=0V$ to $-2.5V$

$V_{gt}=0V$

$V_{gt}=-0.5V$

$V_{gt}=-2.5V$

Drain Voltage (V)

Drain Current (µA)

SiGe

Si

69.0µA

114µA
$V_{gs} \text{ vs } I_{ds}$ 2µm Devices

$V_{ds} = -0.1V$

$V_{t,\text{Si}} = 50mV$

$V_{t,\text{SiGe}} = 380mV$
2µm devices:
Effective low field hole mobility at Vds=-0.1V
94.6cm²/Vs (Si)
156cm²/Vs.(SiGe)
Smaller Devices

Drain Current (µA/µm) vs. Device Channel Length (µm)

Current Enhancement
- 2µm : 65%
- 0.5µm : 14%
- 0.4µm : 20%

$V_{ds} = V_{gt} = -2.5V$
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