Silicon Single-Electron Devices for Logic Applications

NTT Basic Research Laboratories

Yasuo Takahashi

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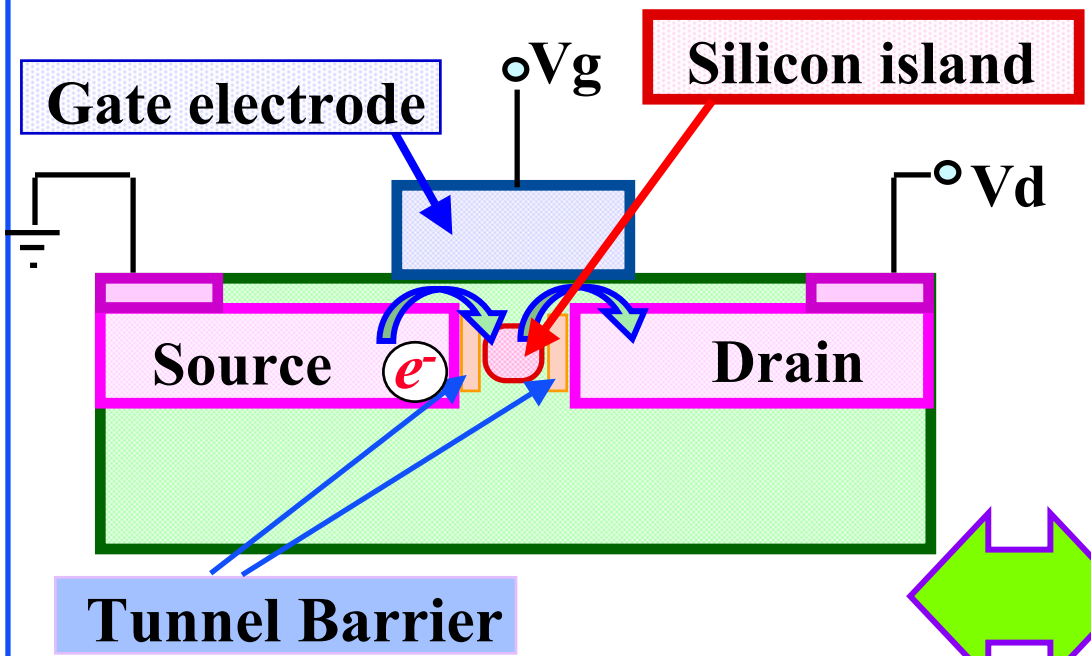
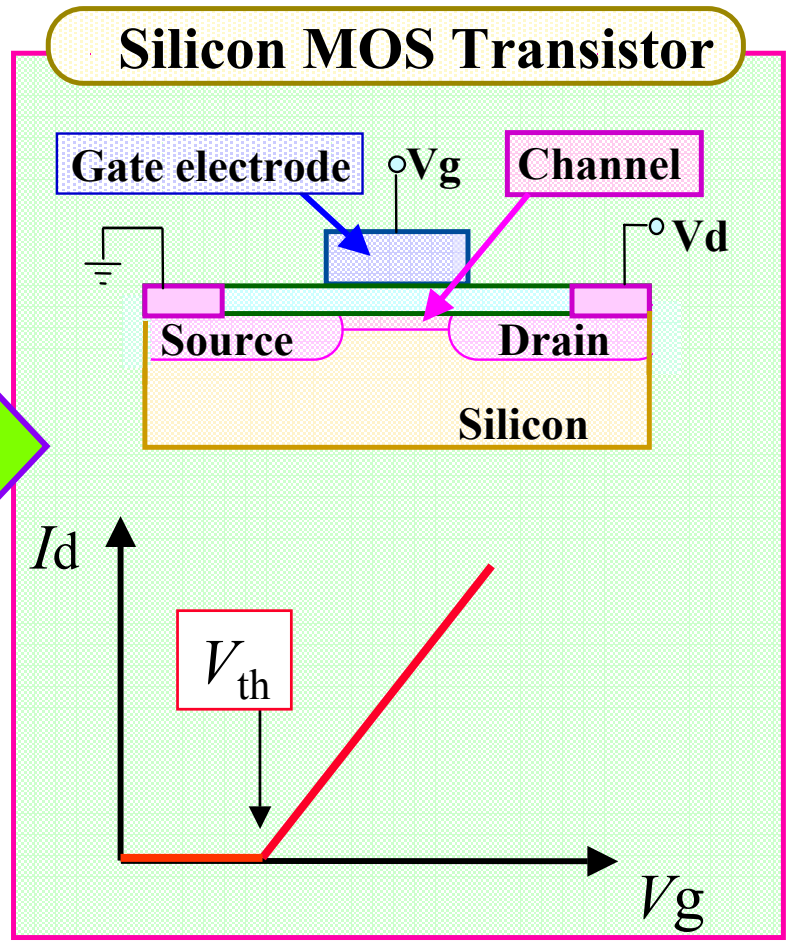
Outline

1. Background
2. Novel Fabrication Procedure for SETs (Pattern-Dependent Oxidation: PADOX)
3. Advantages of SETs made by PADOX
4. Application of SETs for Logic Circuits
   (**Single-Electron Inverter & Adder,**
   Multigate SET, Multiple-Valued Operation)
5. New Device (**Single-Electron CCD**)
6. Summary

Si Single-Electron Transistor

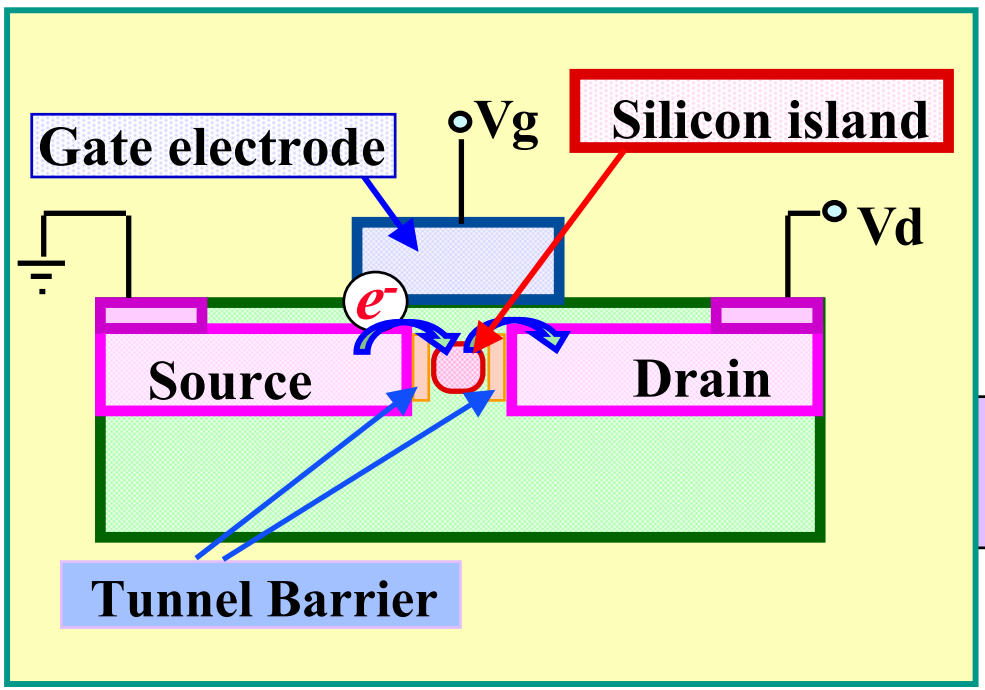


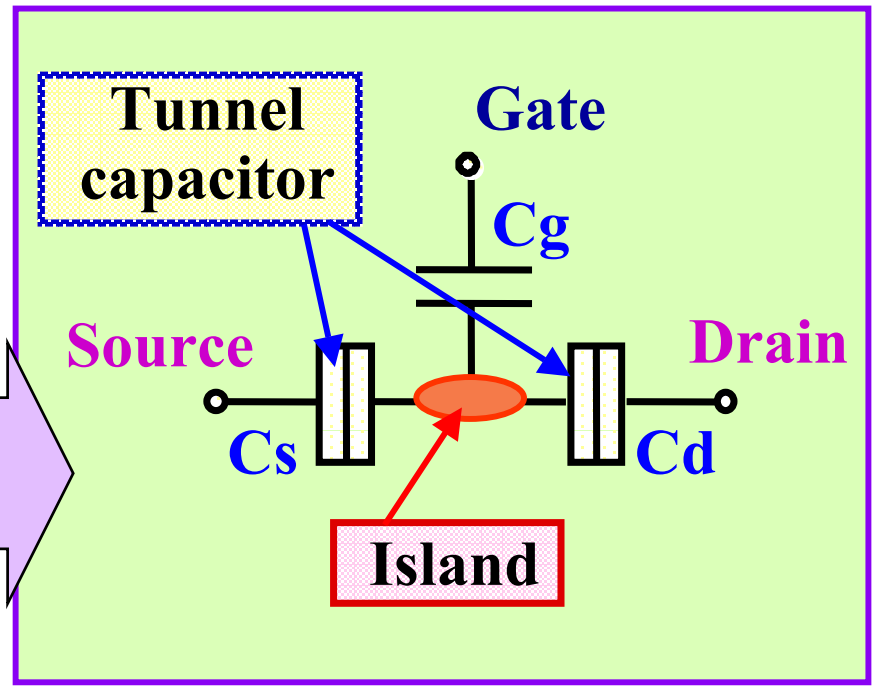


Structure of Si SET

Si single-electron transistor (SET) and MOSFET have similar structure

Equivalent Circuit





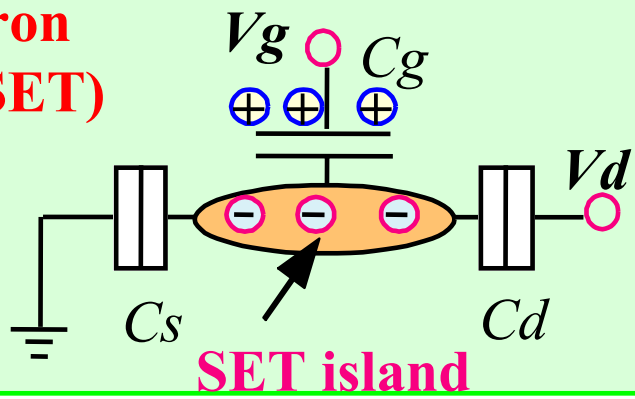
Structure of Si SET

Equivalent Circuit of Si SET

Operation of SET

Single-electron Transistor (SET)

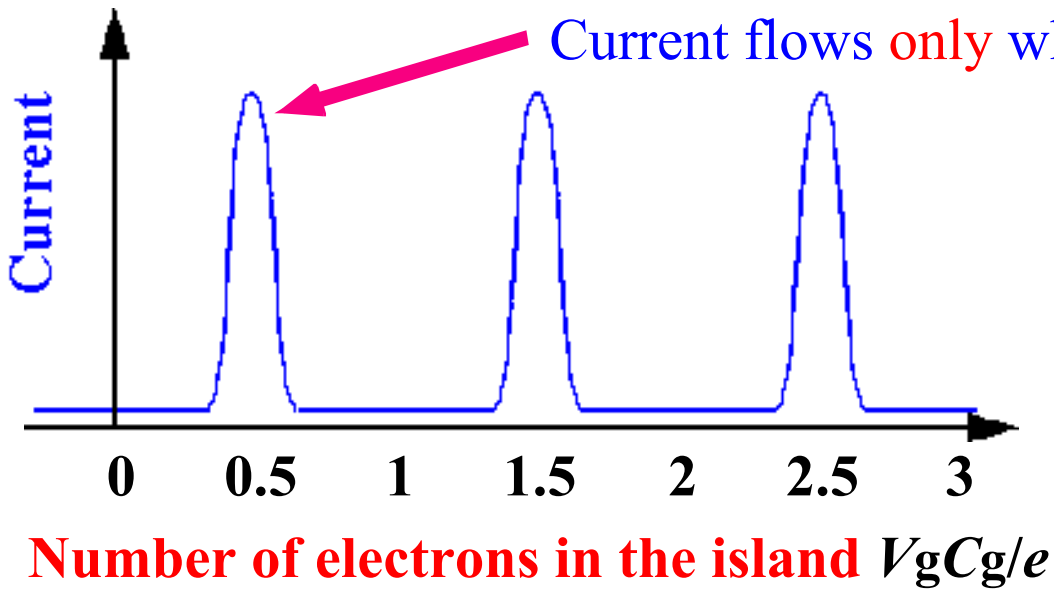
***V*d is small**



The same **number** of electrons

$$Ngate = CgVg/e$$

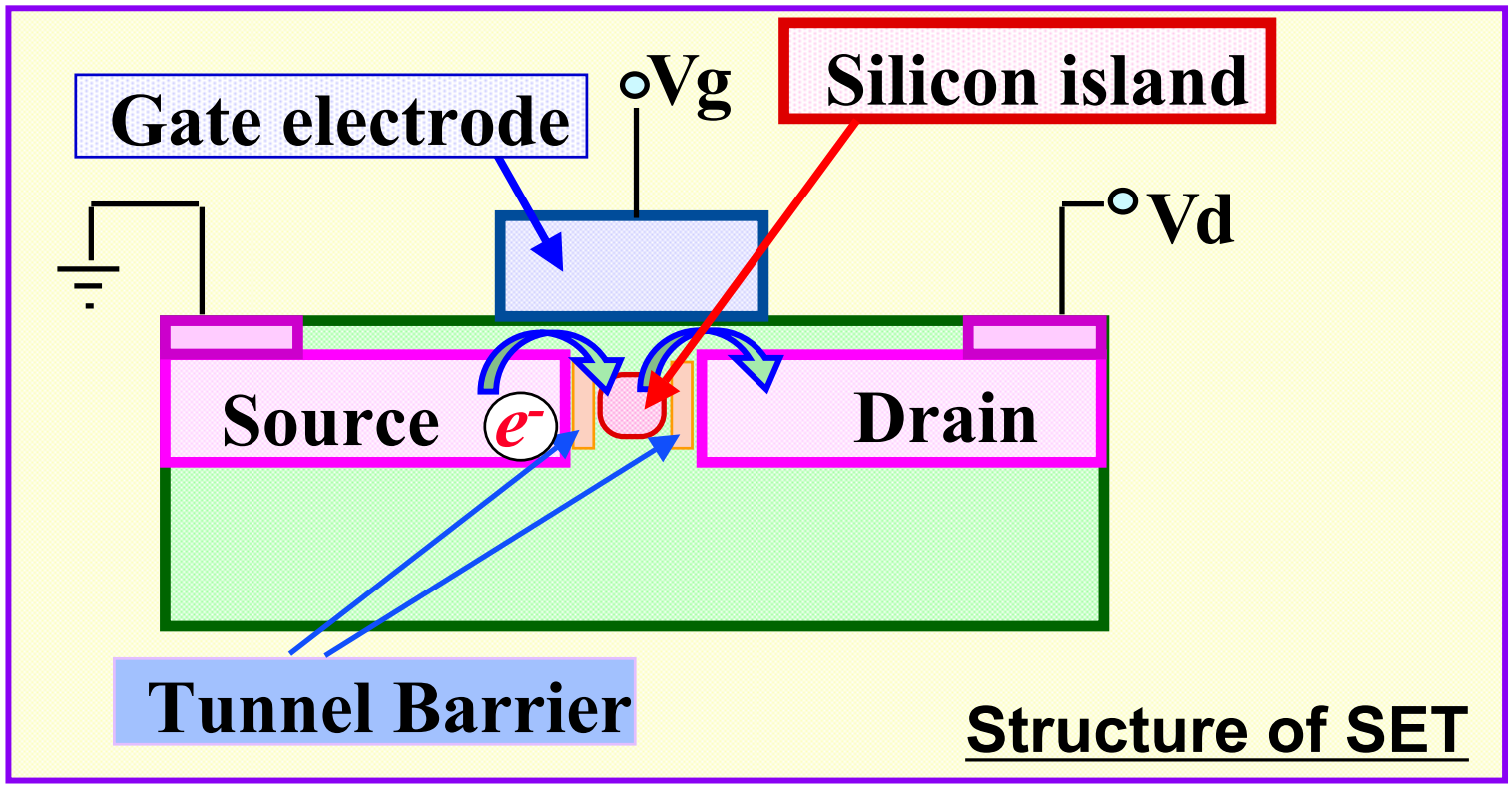
$$Nisland = Integer$$



Current flows only when the number of electrons in the gate is **half-Integer**

Current (Conductance) oscillates as a function of gate voltage (*V*g)

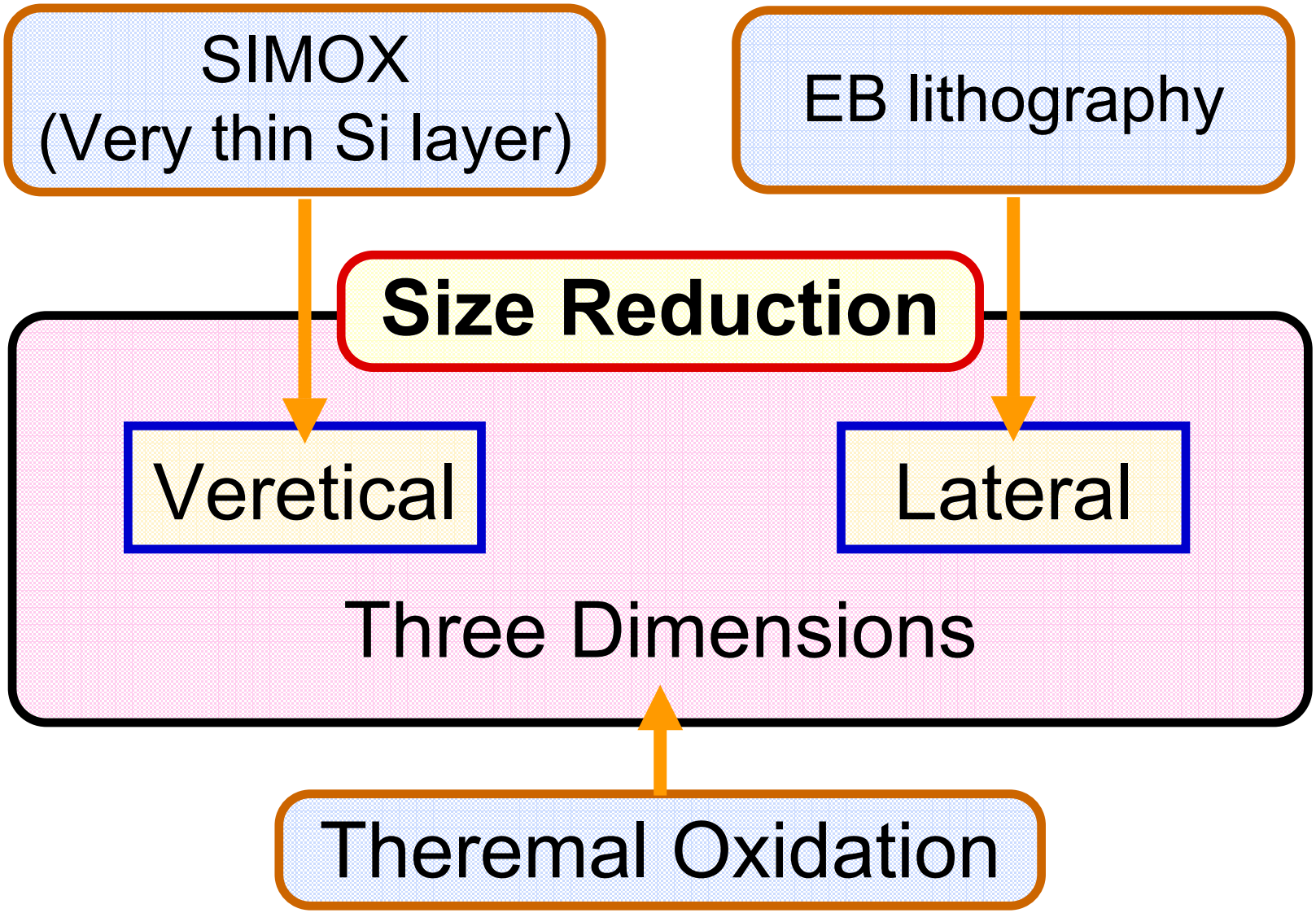
Single-Electron Transistor



Difficulties in fabricating SETs

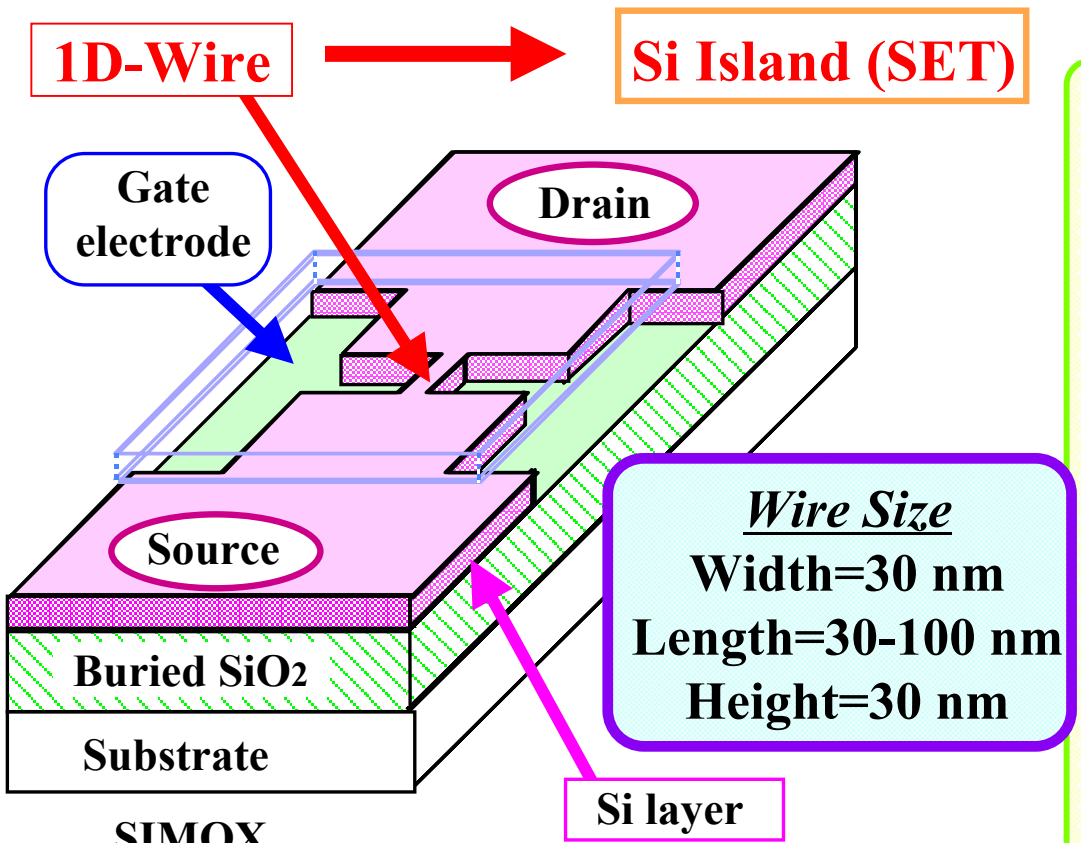
- Formation a small island (~10 nm)
- Attaching two tunnel barriers to the island

Strategy for Size Reduction

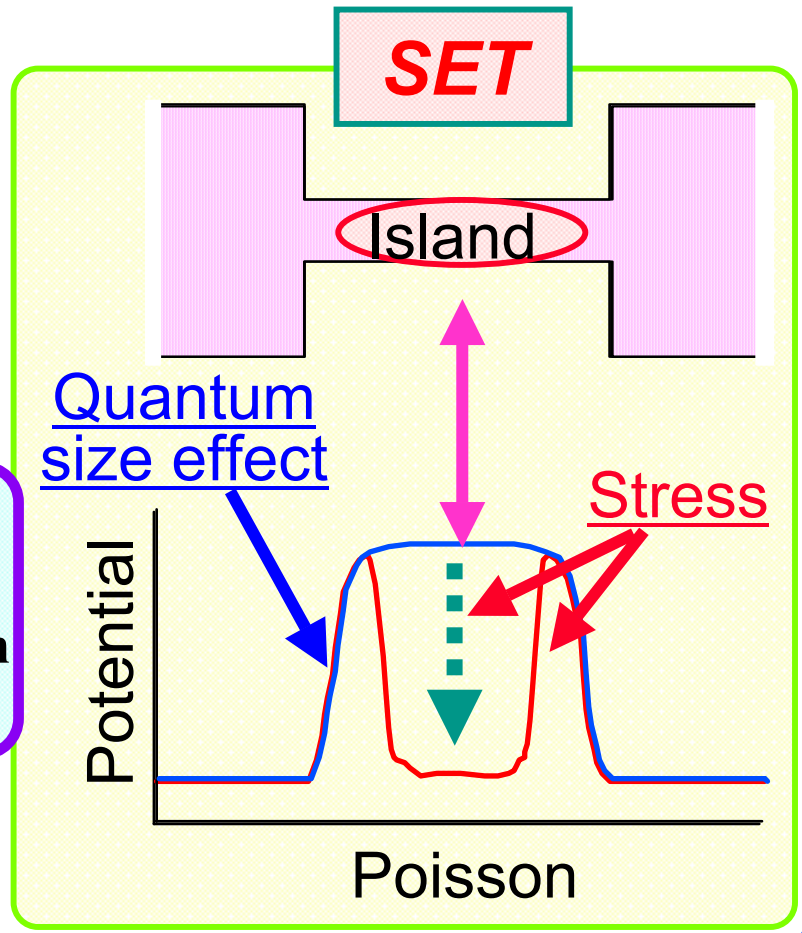


Pattern-Dependent Oxidation (PADOX)

Self-aligned formation of a single Si island



(Y. Takahashi, IEDM 1994)



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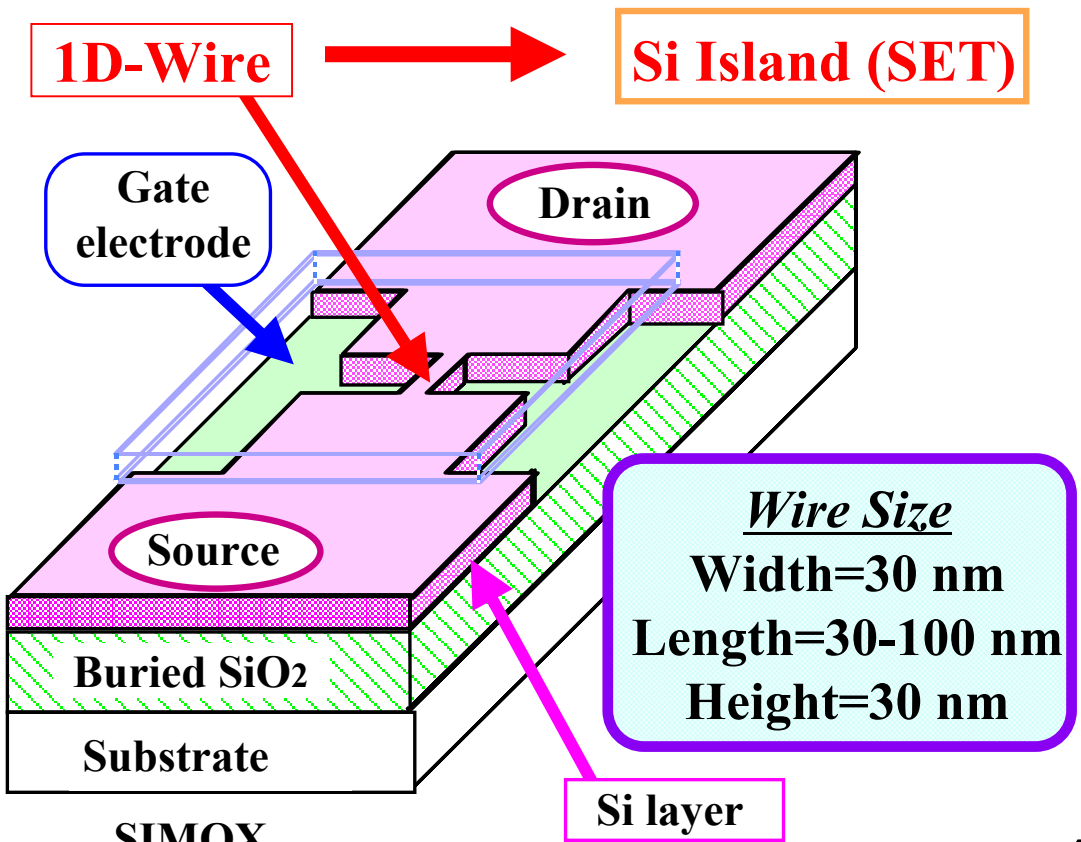
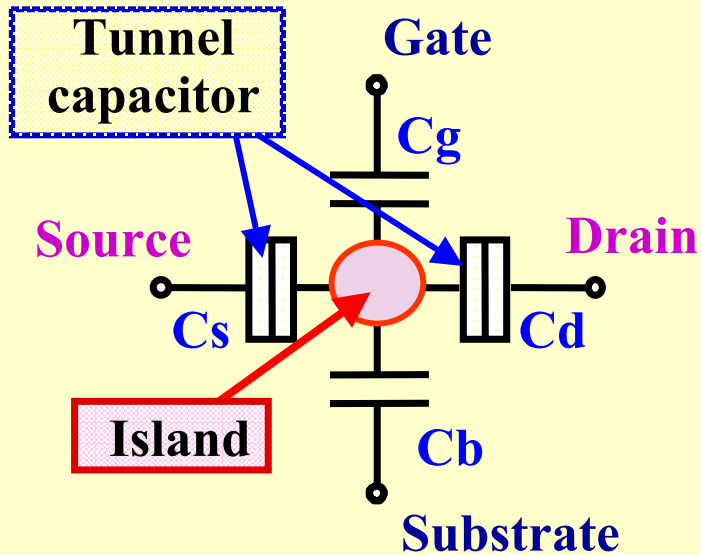


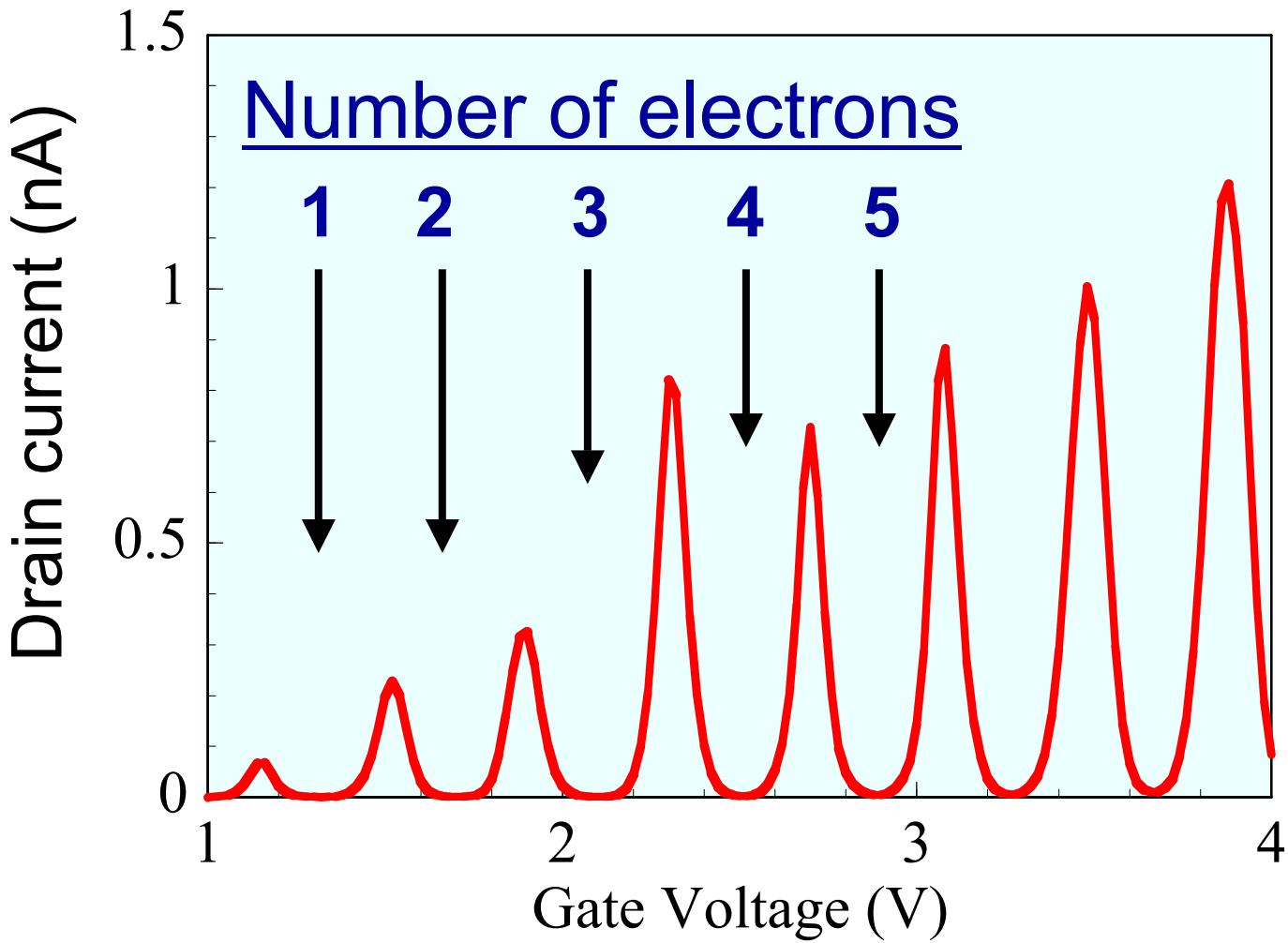
Wire Size
Width=30 nm
Length=30-100 nm
Height=30 nm



"Single-Electron Transistor (SET)"

(Y. Takahashi, IEDM 1994)

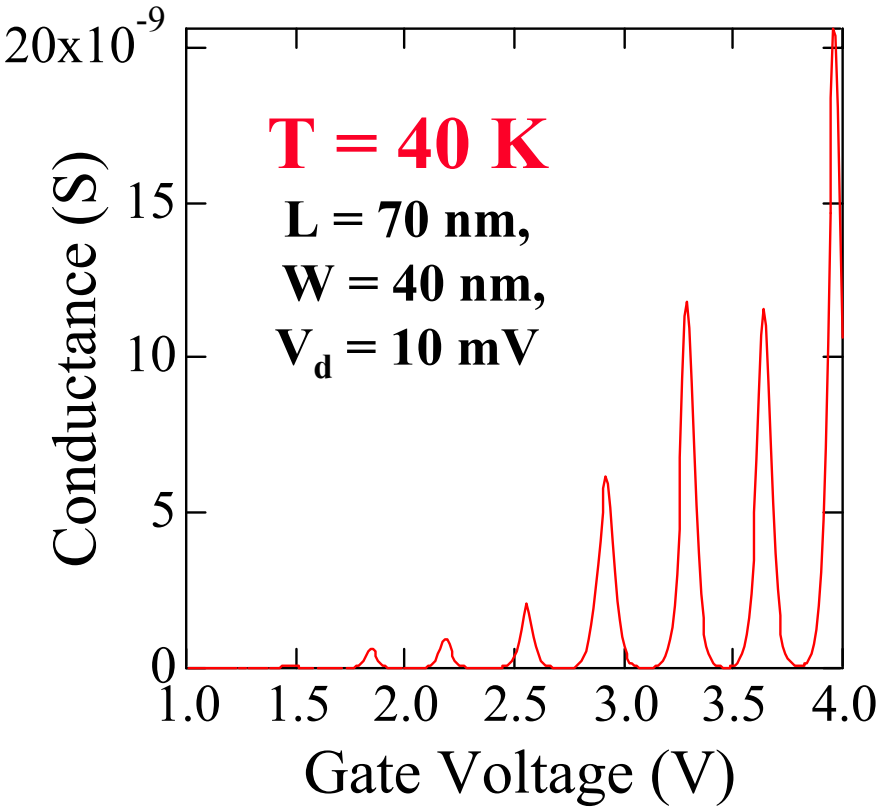
I-Vg Characteristics of Si SET

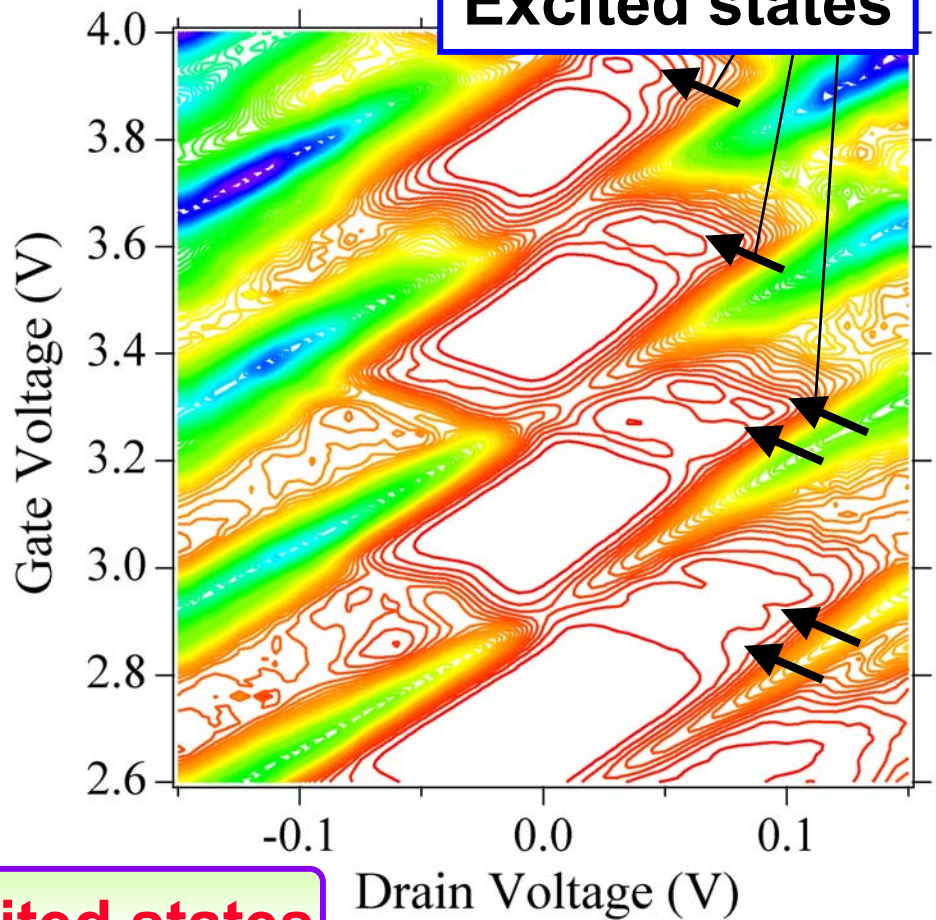


T = 40 K

L = 70 nm,
W = 40 nm,
V_d = 1mV

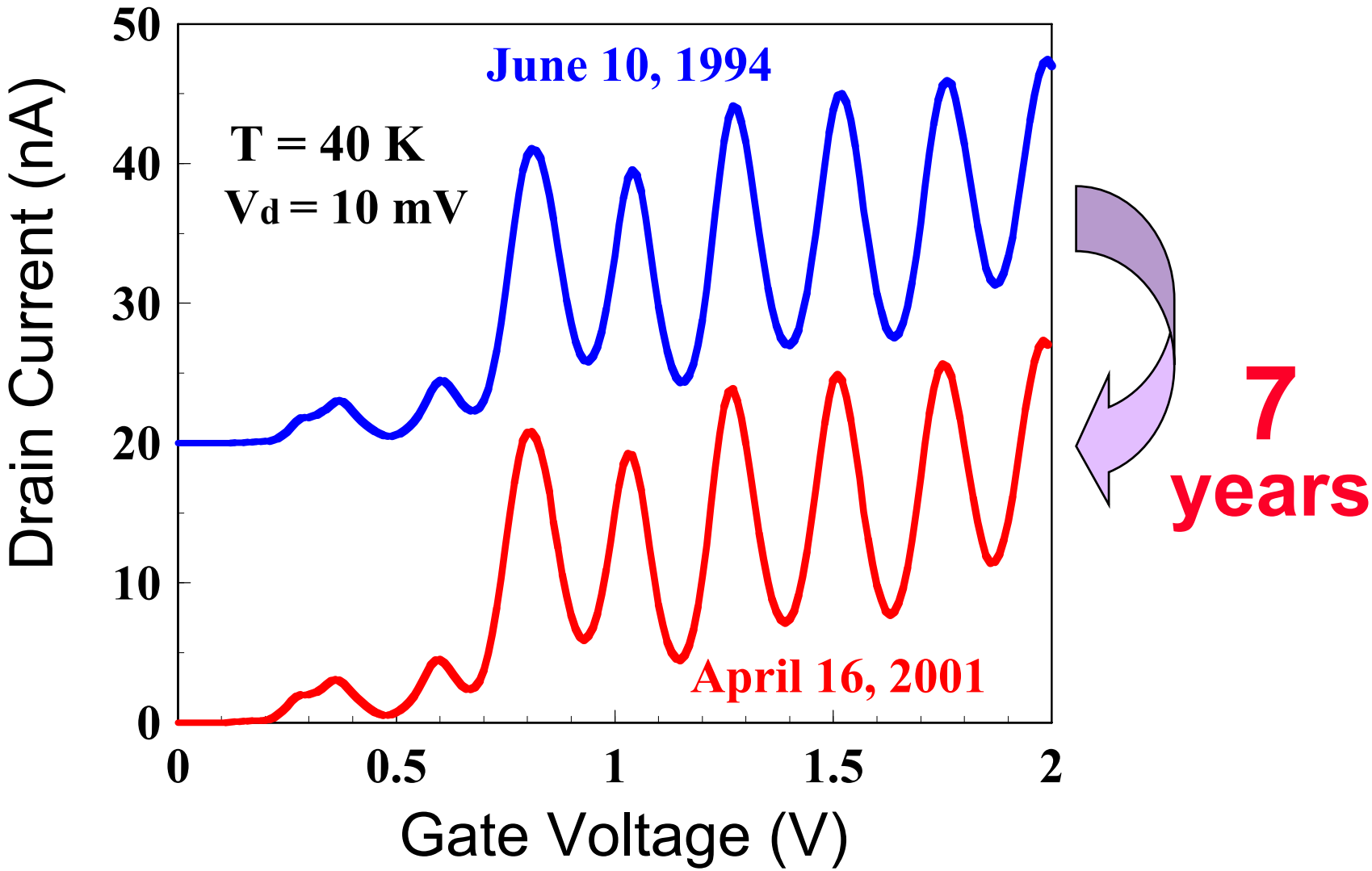
Characteristics of Si SET Fabricated by PADOX



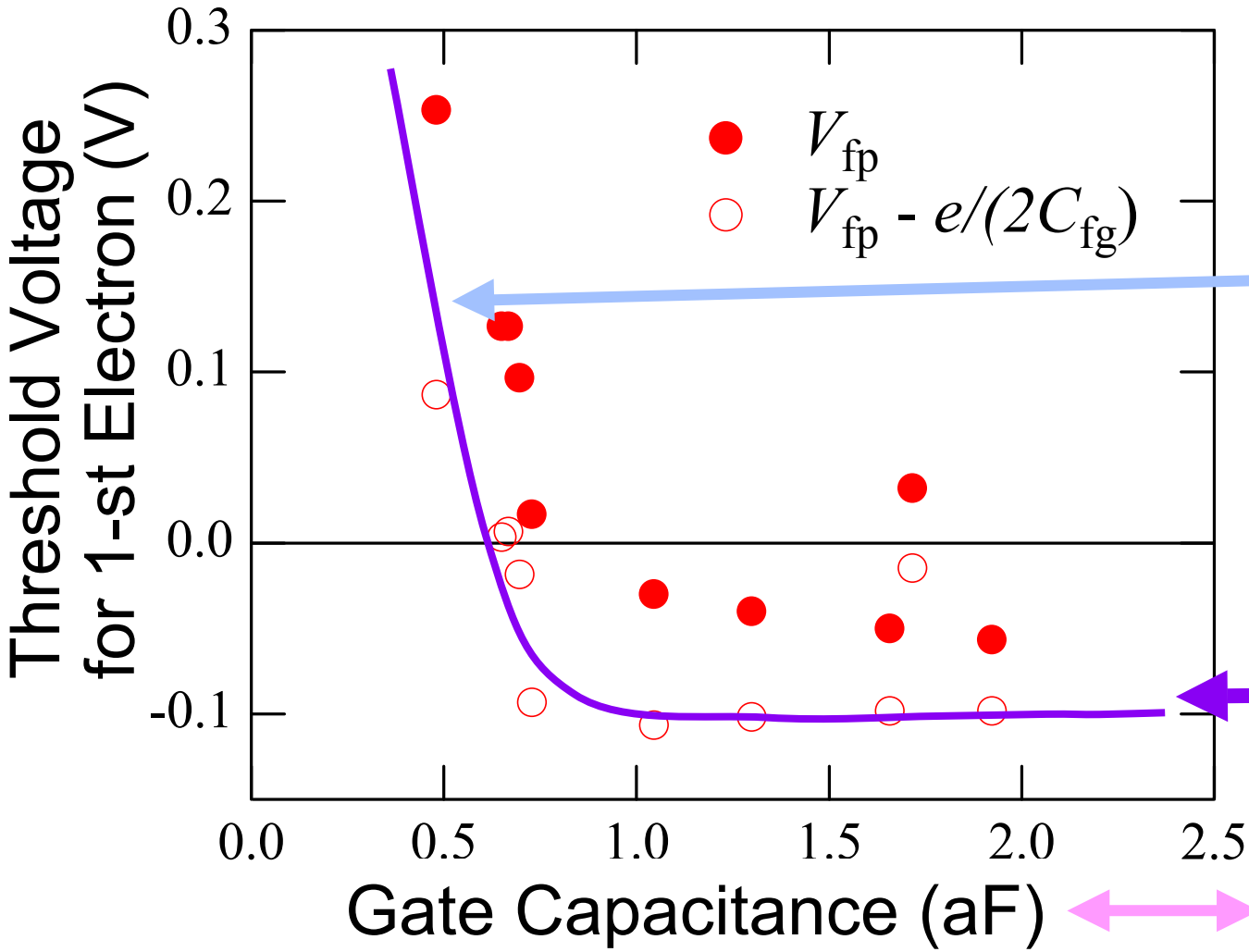


large charging energy and exited states

Stability of I-Vg Characteristics



Threshold Voltage for 1-st Electron



Increase by quantum size effect

Almost constant & -100 mV

Island size

Advantages of Si SET (PADOX)

- **Small Total Capacitance** ~1 aF (~300 K)
  Integration of Small Islands
- **Reproducible** and **Controllable** Fabrication Process (**Capacitance** and **Conductance**)
- Very **Stable Operation like a MOSFET**
  (**No** Effects of **Offset Charge**)
- **Same Process** as for **Si MOS LSI**/SOI

Logic Applications of Si SET

Logic Applications of Si SET

Special Features of SET

Oscillatory I-Vg Characteristics

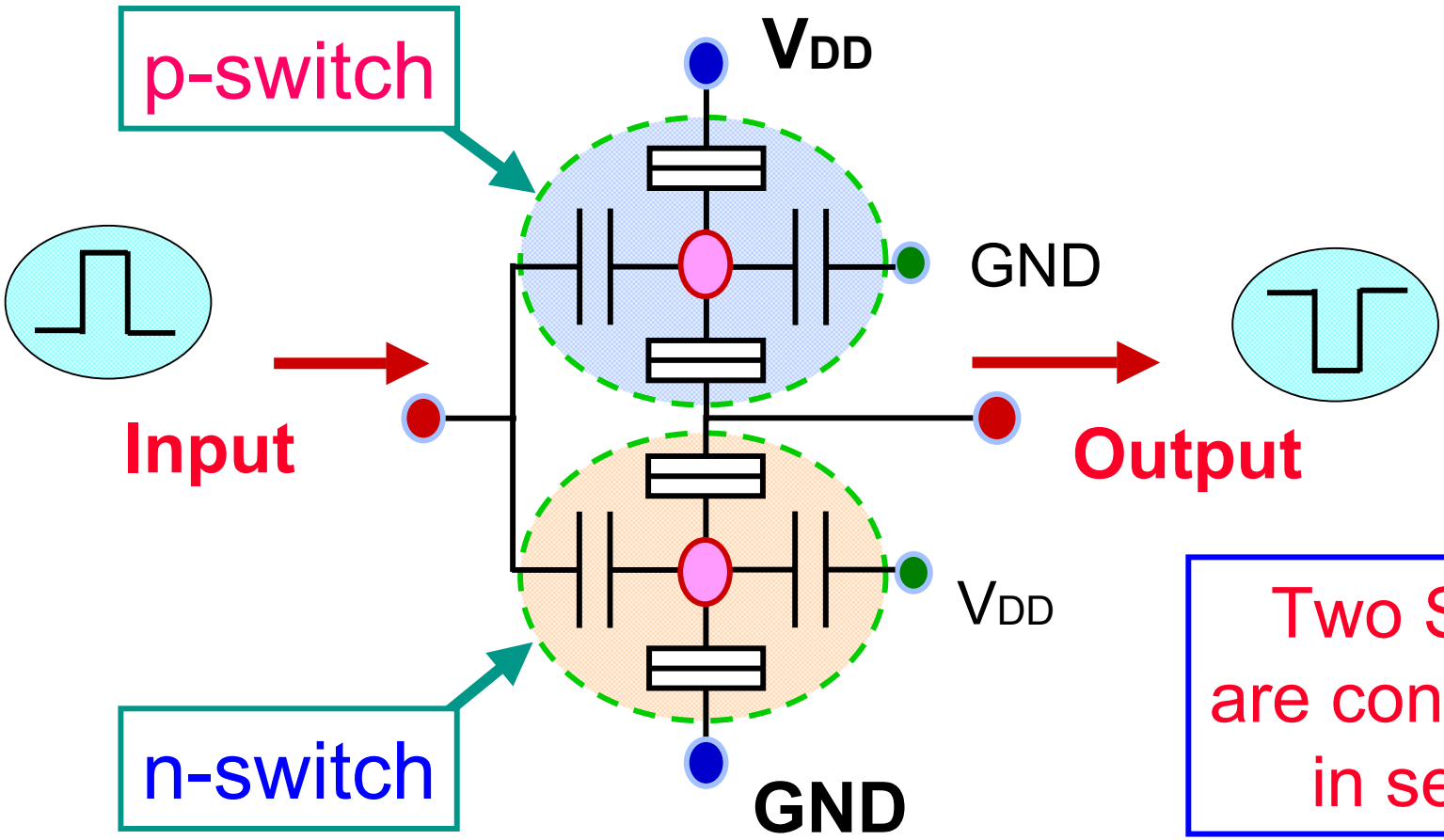
- Operattion as a p-type and n-type Switch
  (CMOS-type Inverter, Adder)
- Multiple-valued Operation
  (Multiple-valued memory, Quantizer)

Multigate Capavility

- Gate-Level Summation
  (X-OR gate, Multi-bit Adder)

CMOS-type of SET Logic

CMOS-type Single-Electron Inverter

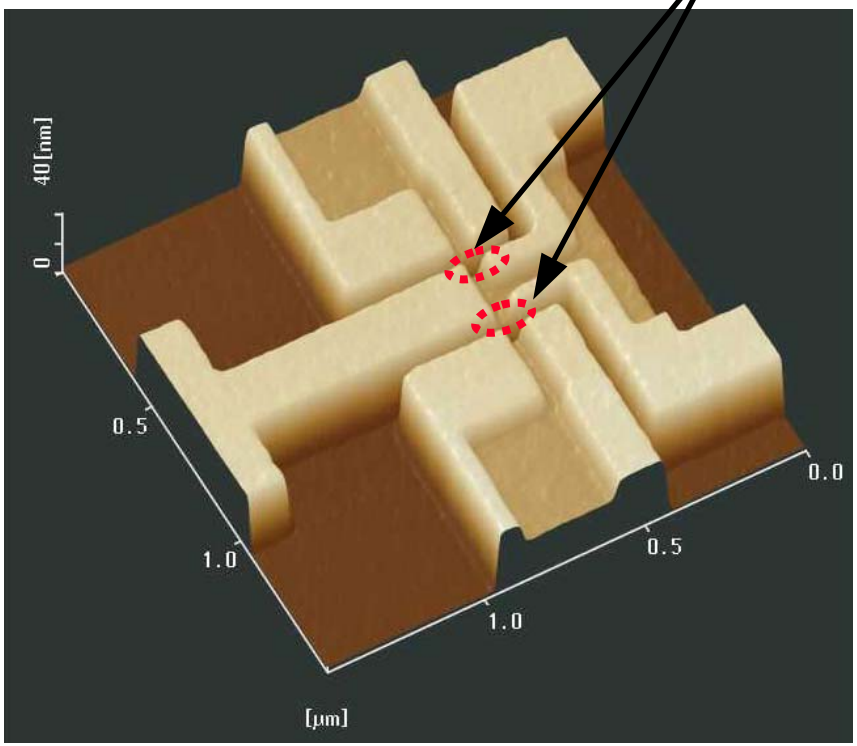


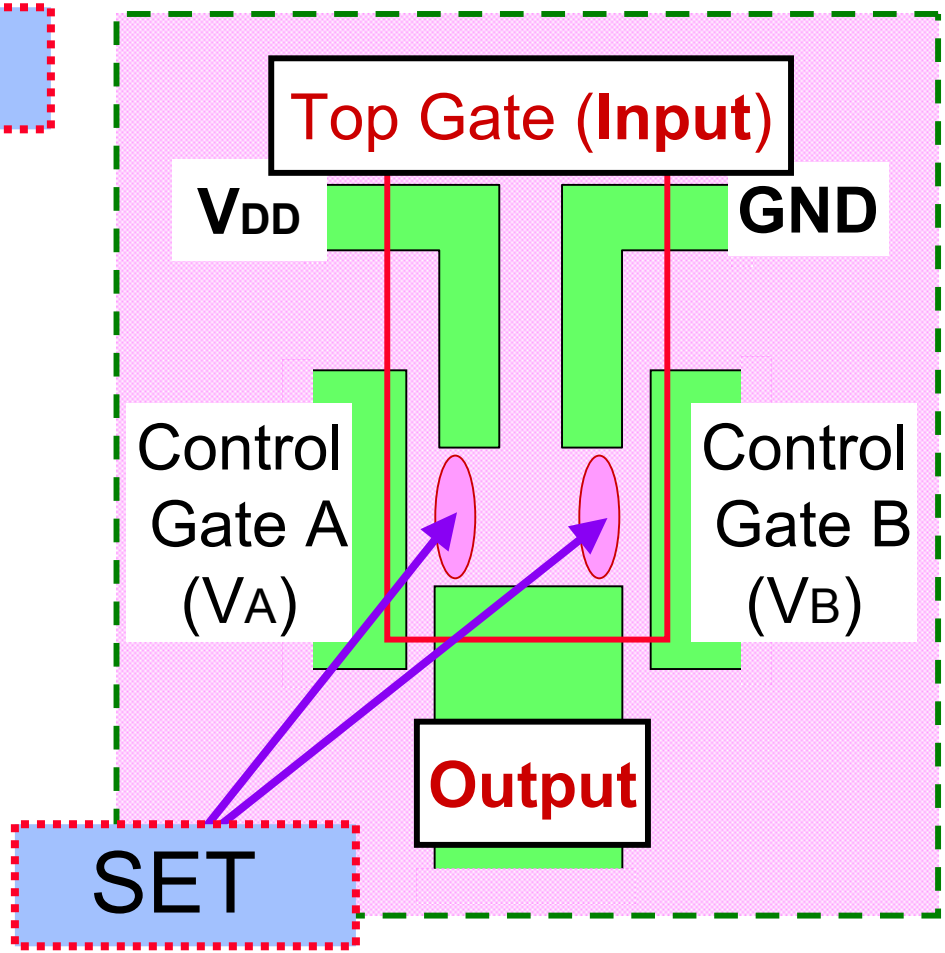
Two SETs are connected in series

J. R. Tucker, JAP, 72, 4339 (1992).

SETs Connected Series (V-PADOX)

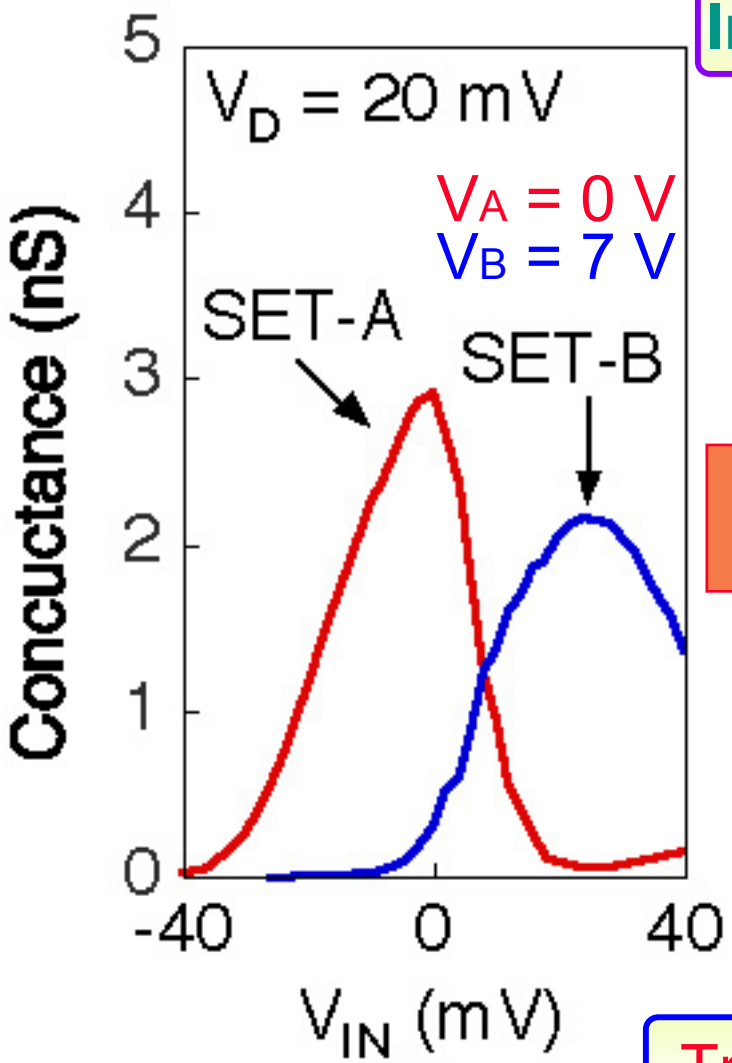
AFM Image



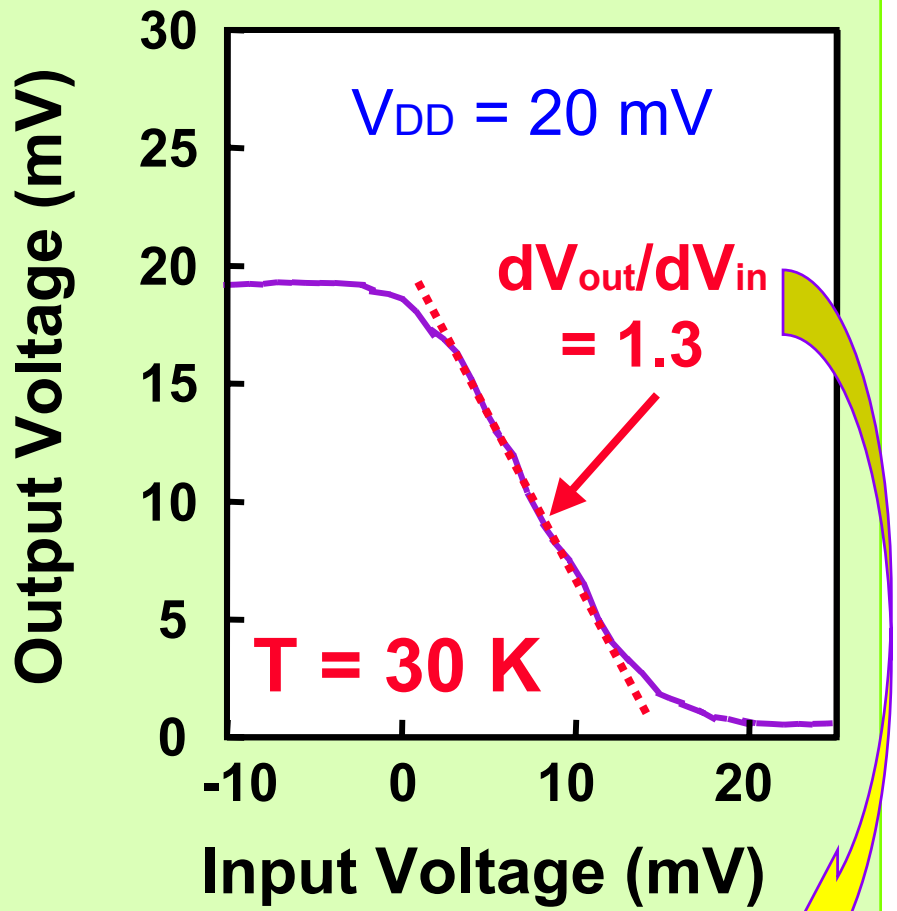


Y. Ono et al., APL, 76, 3121 (2000).

Inverter Operation



Input-Output Transfer Characteristics



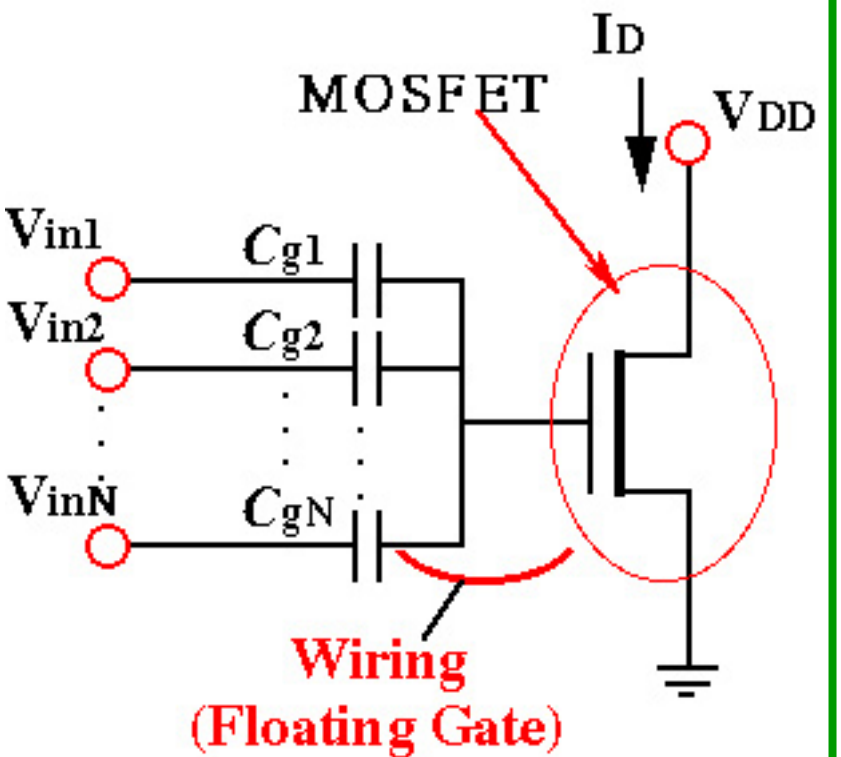
Transfer of signal & CMOS-type logic

Y. Ono et al., APL, 76, 3121 (2000).

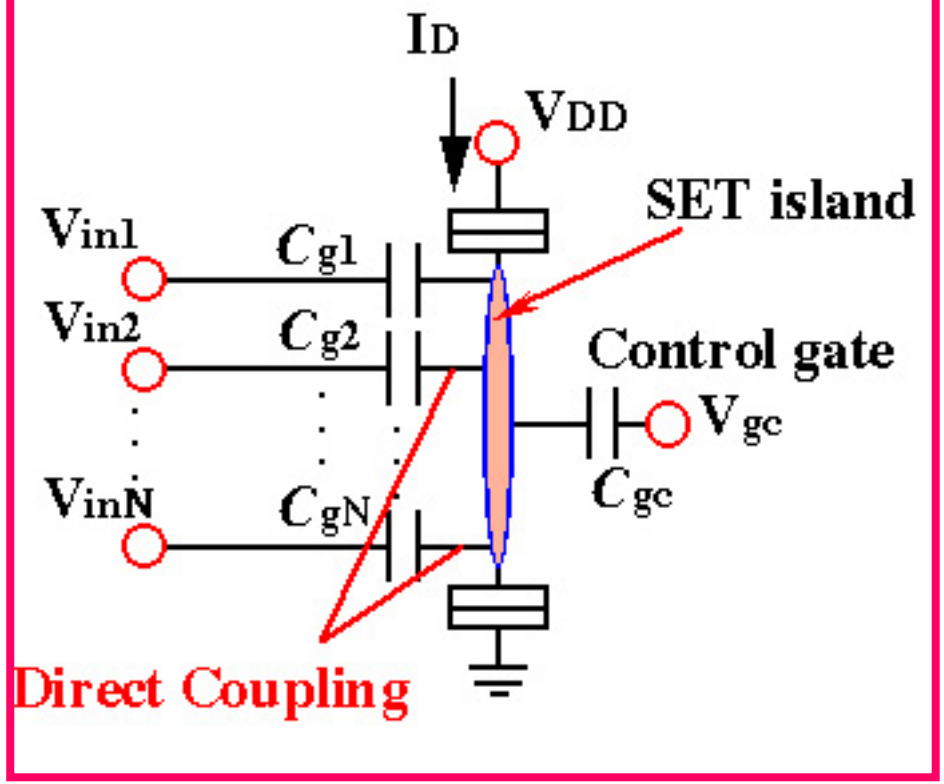
Multiple-Gate Si SET

Multi-gate MOSFET & SET

Multi-gate MOSFET



Multi-gate SET

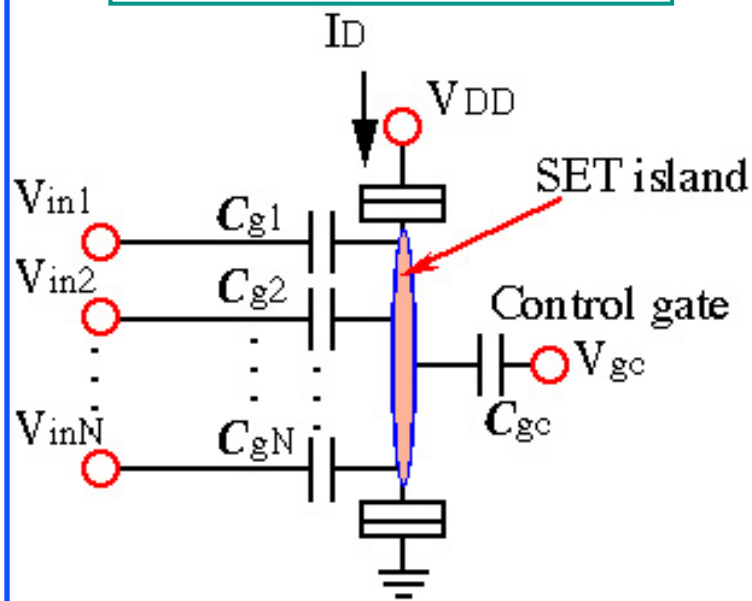


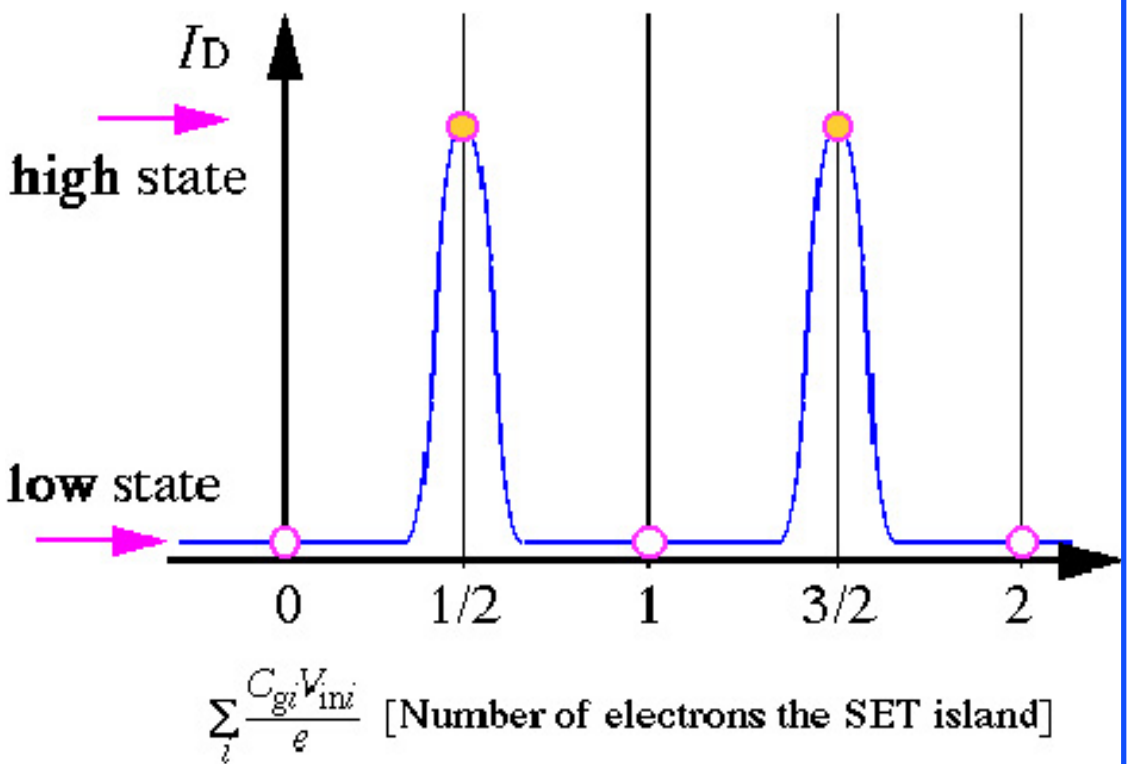
T. Shibata et al., IEEE Tras. ED, 39, 1444 (1992).

Y. Takahashi et al., APL, 76, 637 (2000).

Multi-gate SET (X-OR gate)

Multi-gate SET





$C_{gi} = C_{g0}$ (I =1,2 … N)

$V^{H}_{ini} = e/2C_{g0}$

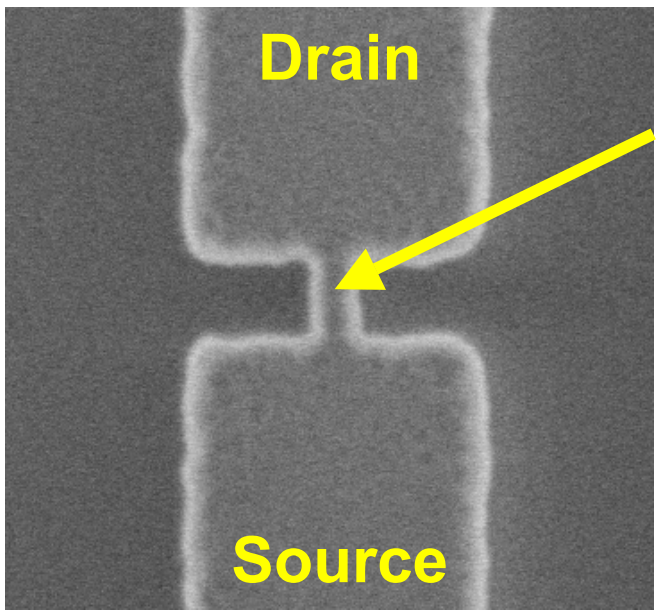
Even number of *High-gate* **Low** states

Odd number of *High-gate* **High** states

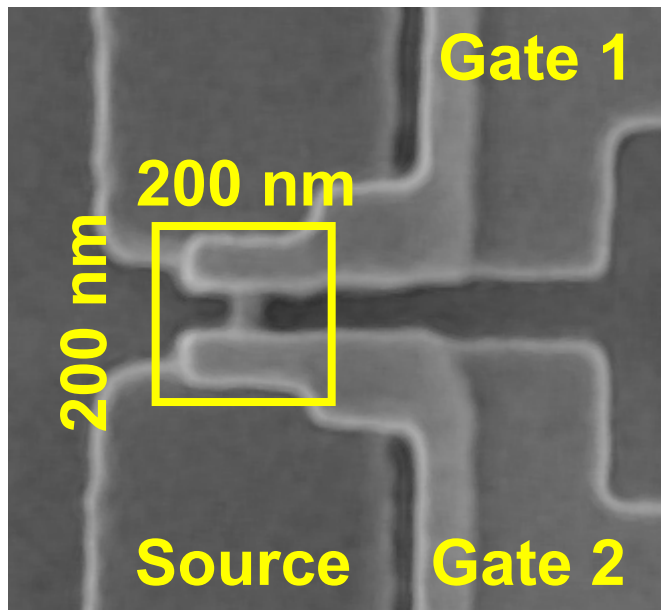
Y. Takahashi et al., APL, 76, 637 (2000).

SEM Images of Dual-gate SET

Dual-gate SET **(Parallel Gates)**



SET Island

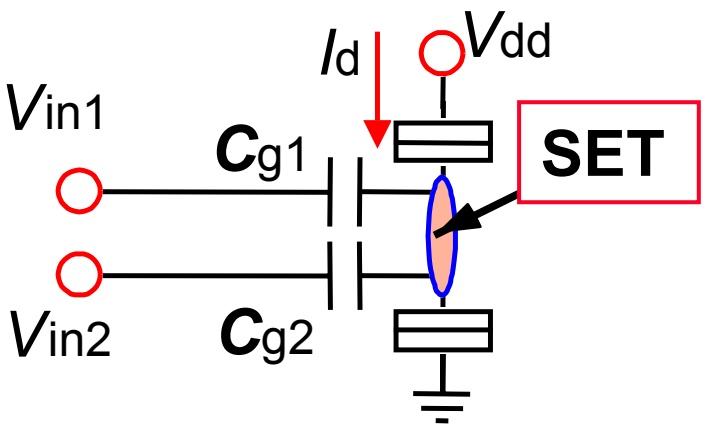


Si wire
(SET)

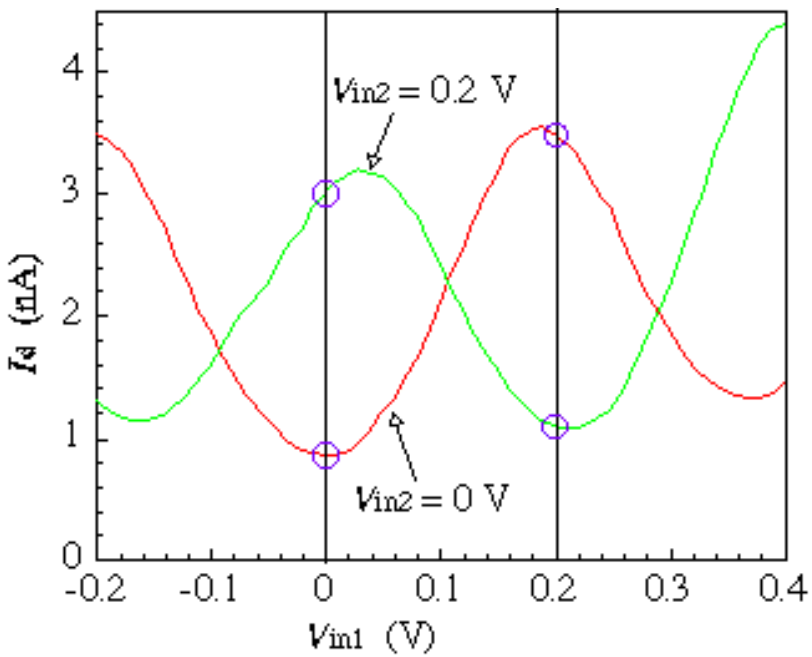
Ultra fine parallel gate
(XOR Gate)

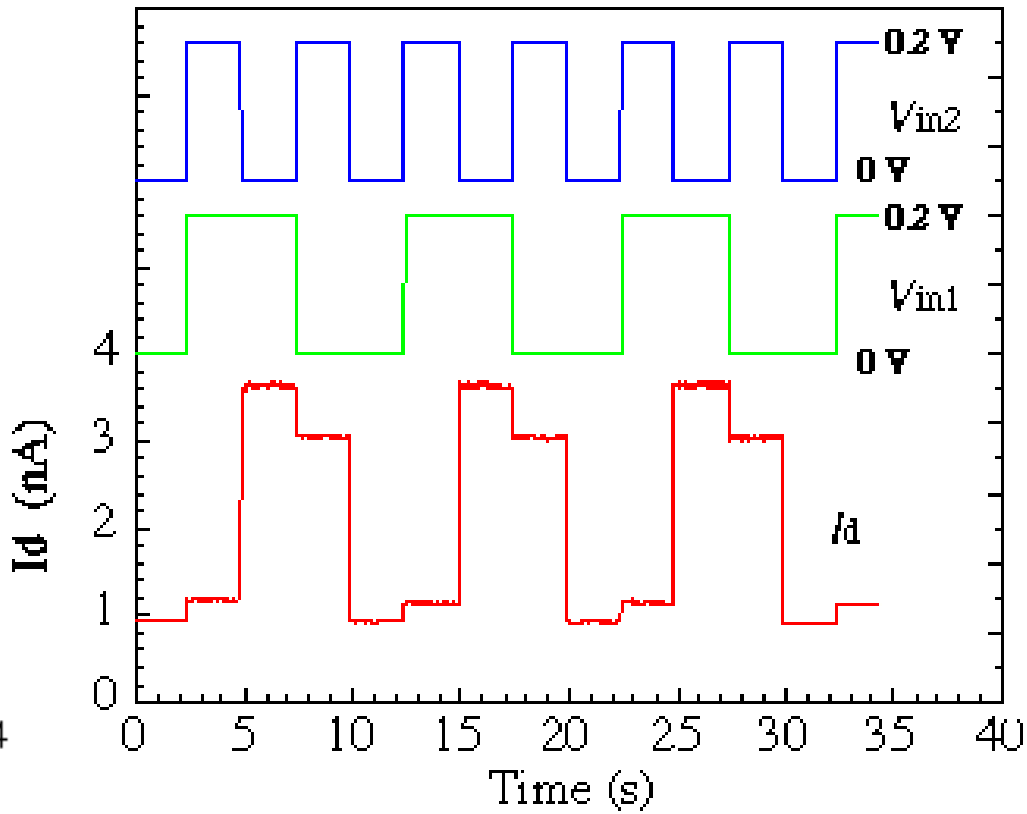
Y. Takahashi et al., APL, 76, 637 (2000).

XOR Operation of Dual-gate SET



C_{g1}= 0.42 aF
C_{g2}= 0.36 aF



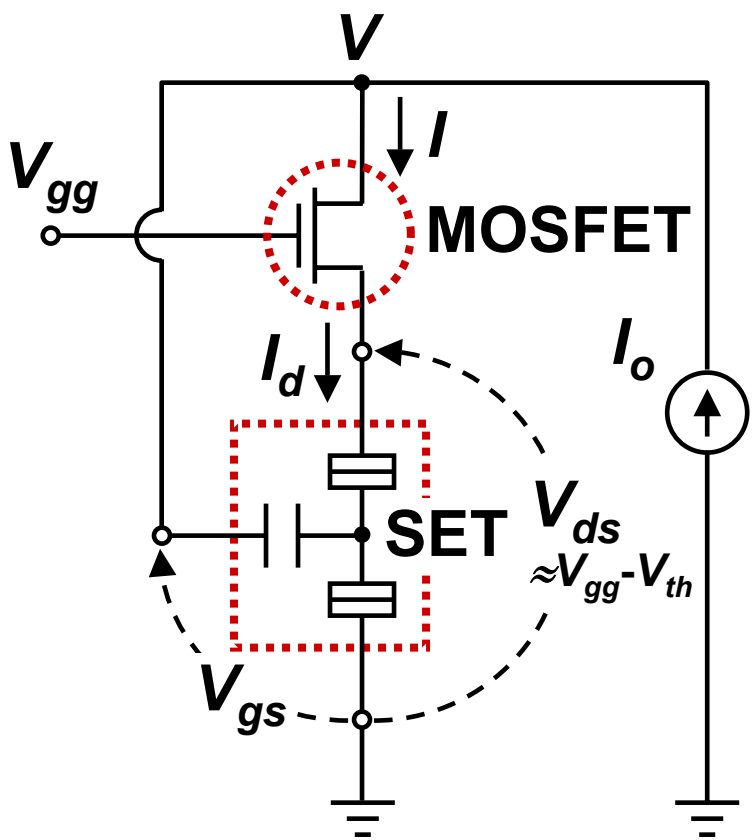


Y. Takahashi et al., APL, 76, 637 (2000).

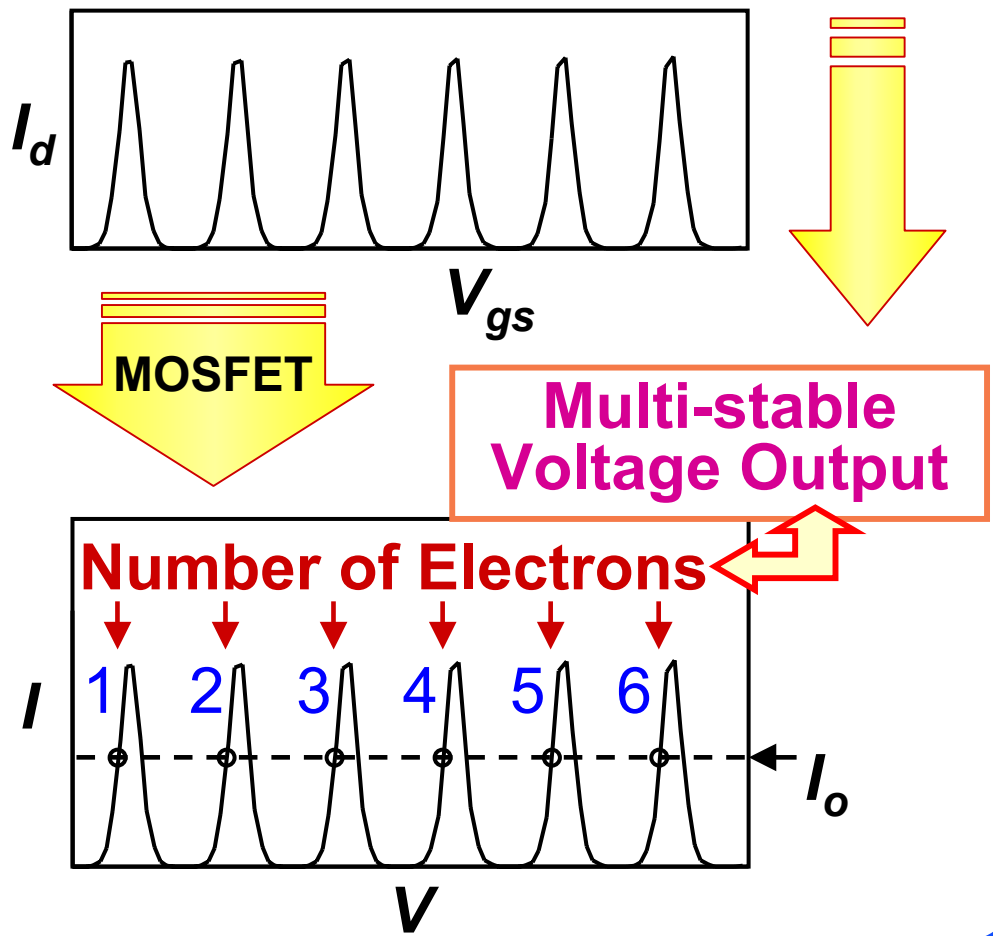
Multiple-Valued Application of SET

Multiple-Valued Application
Corresponding to Electron Number

Multiple-valued Memory

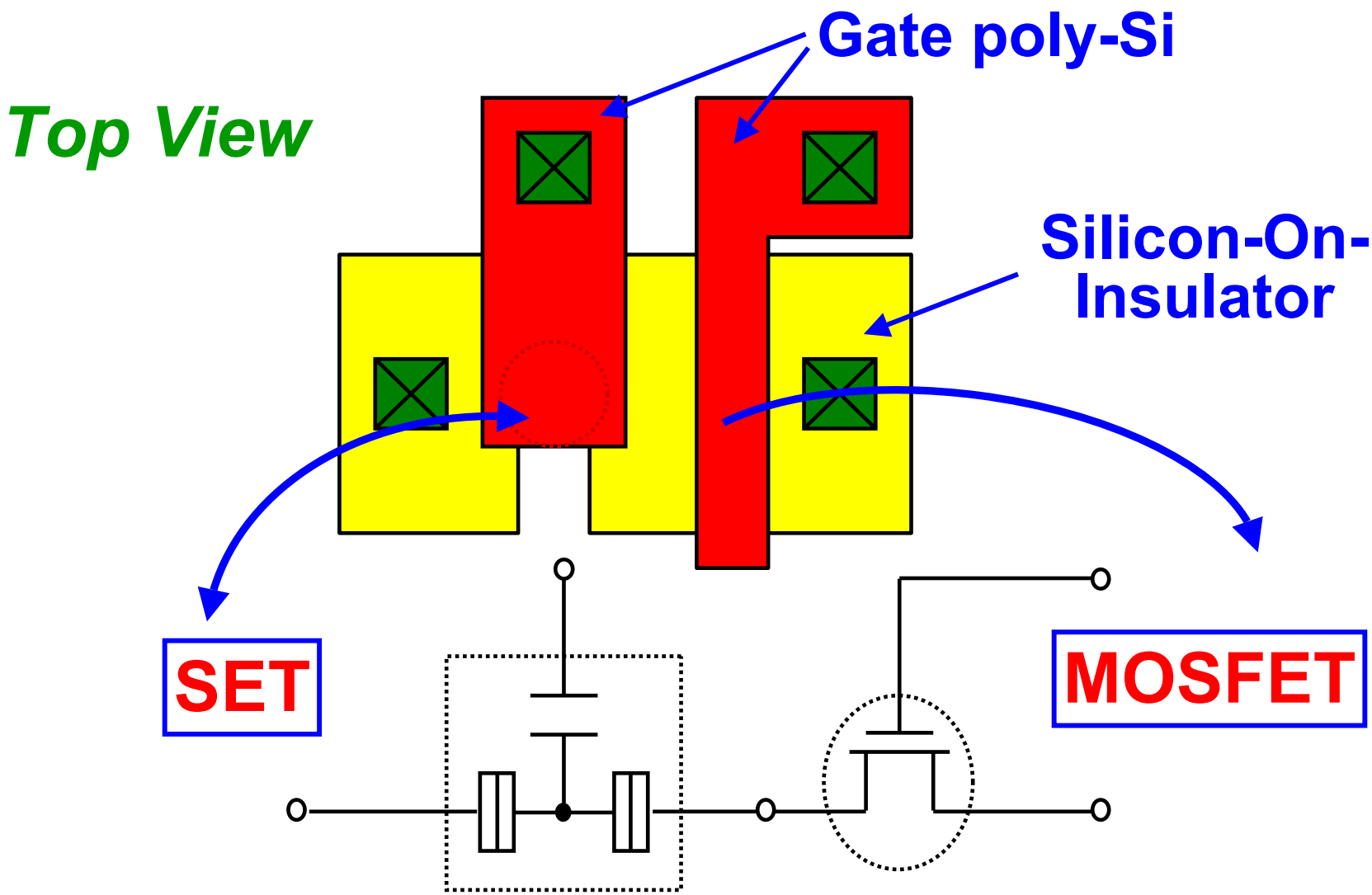


I-Vg charac. (Current Output)



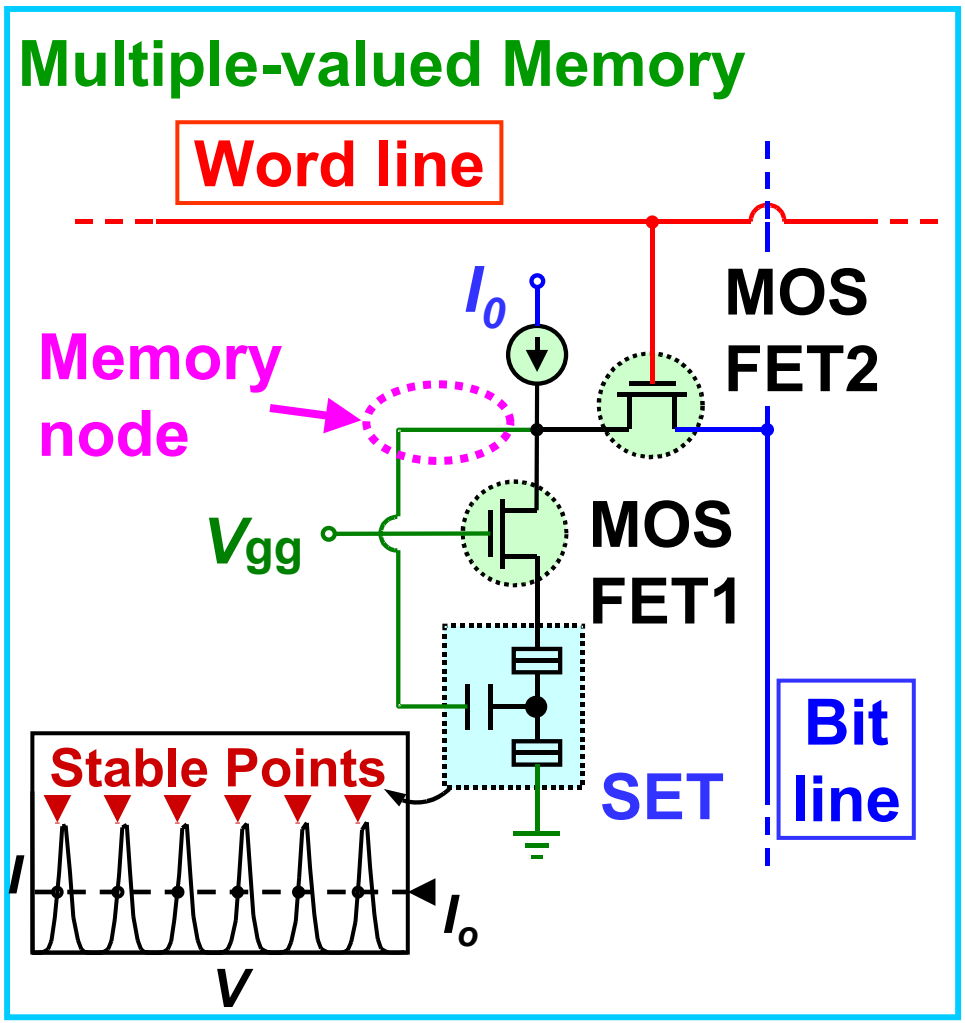
H. Inokawa et al., DRC, (2001).

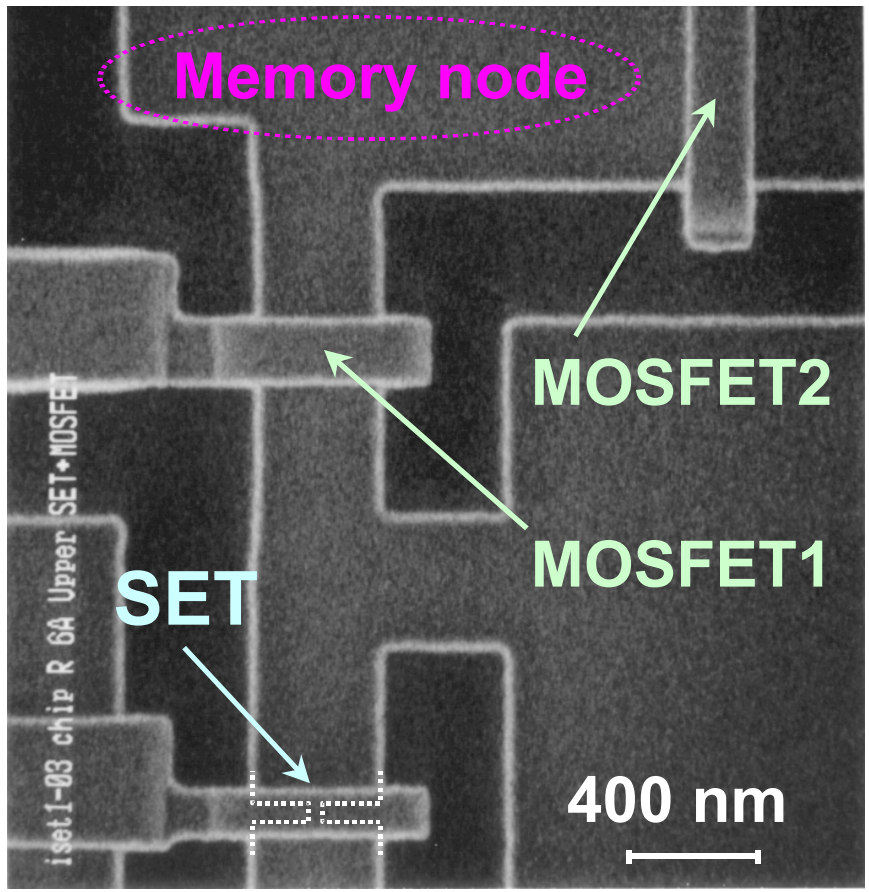
Integrated SET and MOSFET



H. Inokawa et al., DRC, (2001).

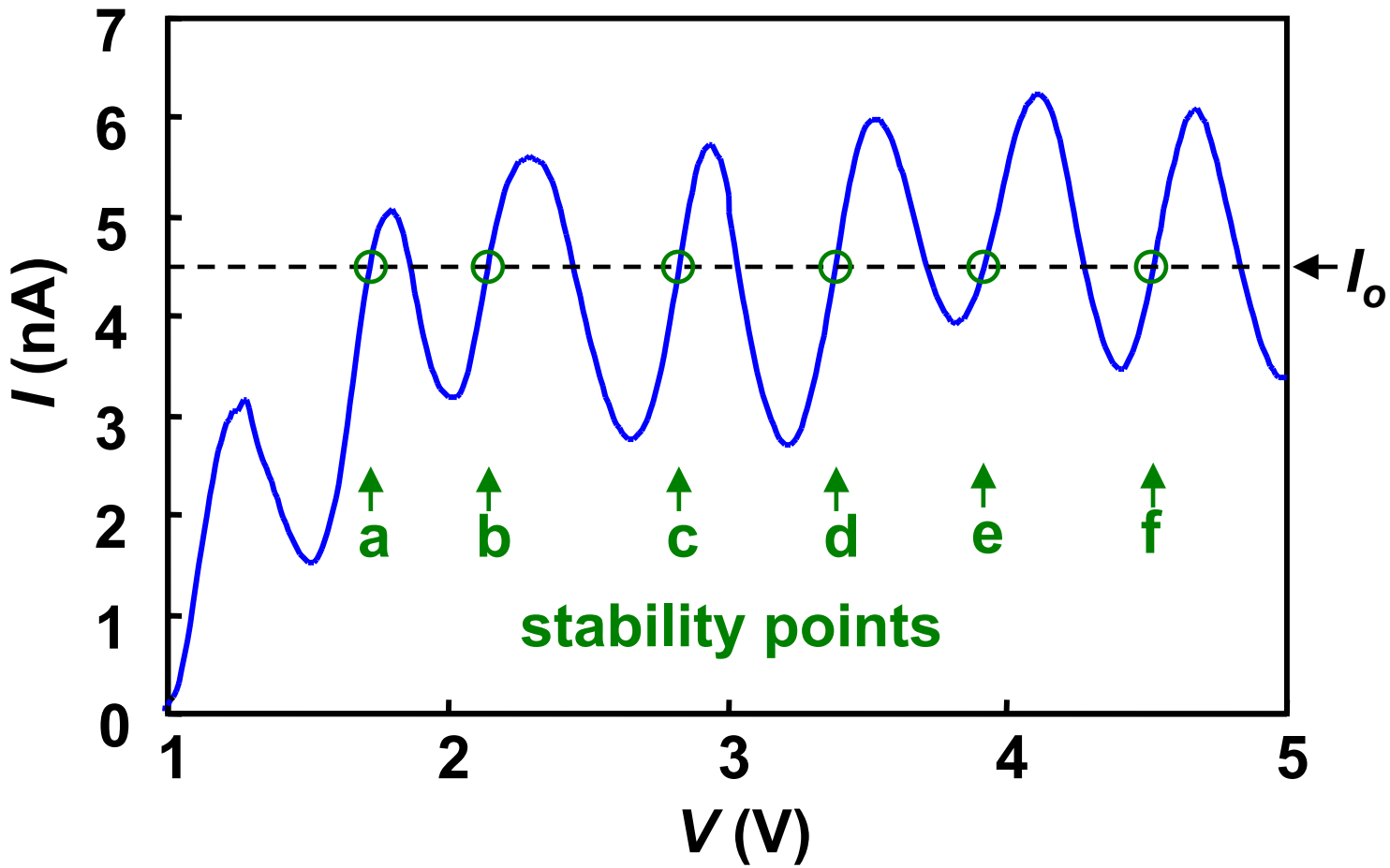
Multiple-Valued Application
Corresponding to Electron Number





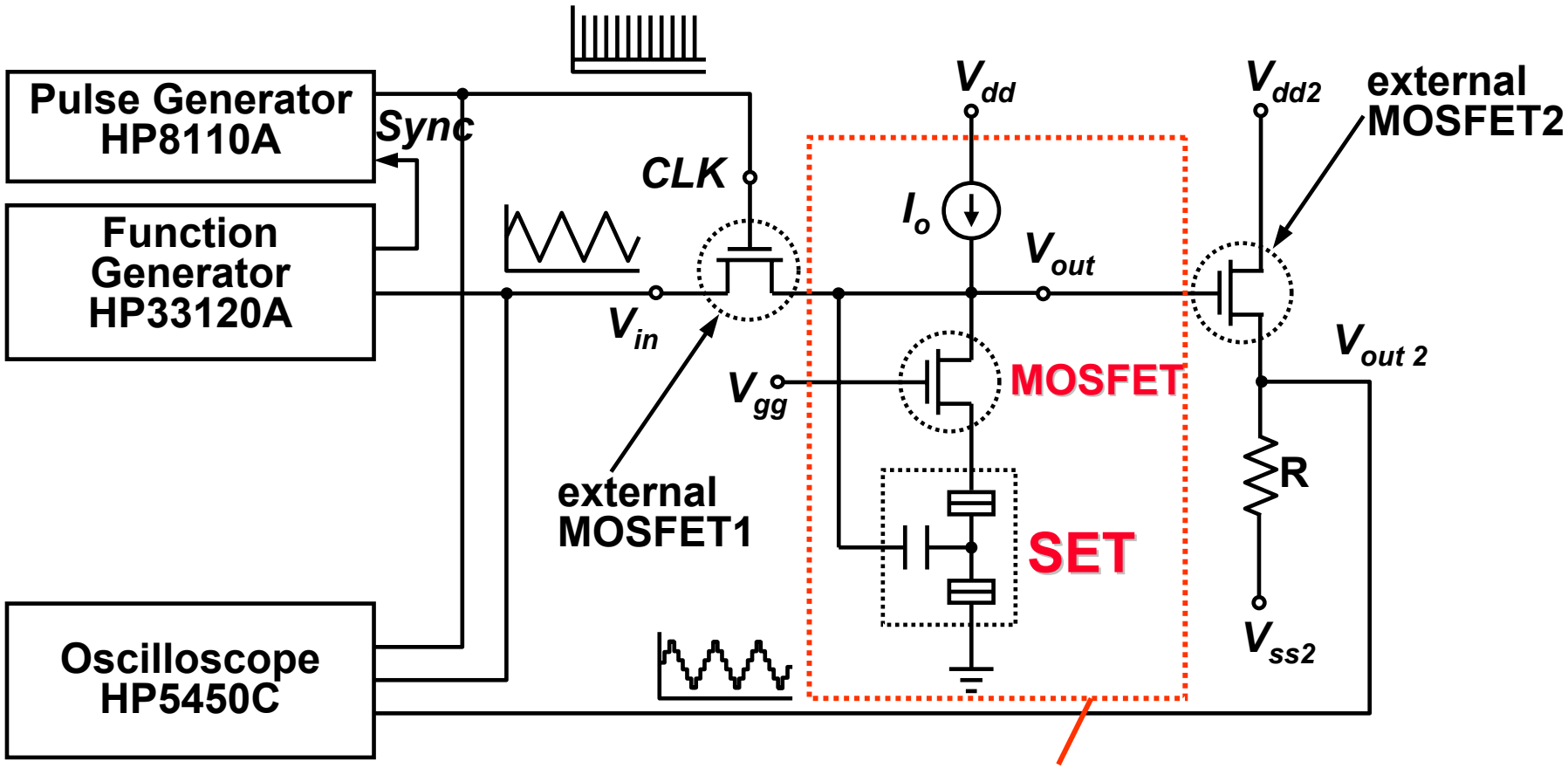
H. Inokawa et al., DRC, (2001).

SET-MOSFET 2-terminal I-V



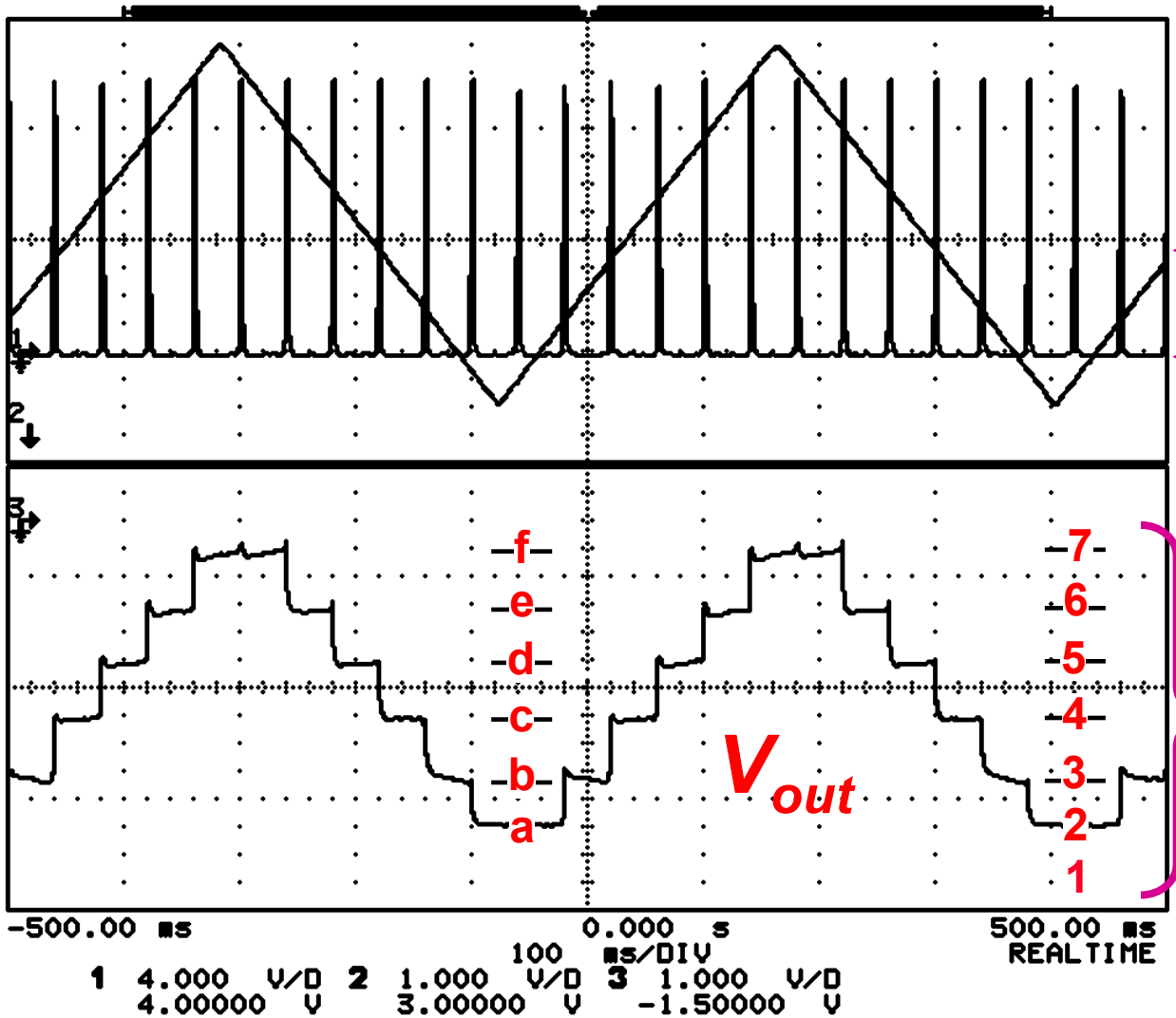
H. Inokawa et al., DRC, (2001).

Single-Electron Quantizer
(Multiple-Valued Operation)



H. Inokawa et al., IEDM, (2001).

Single-Electron Quantizer

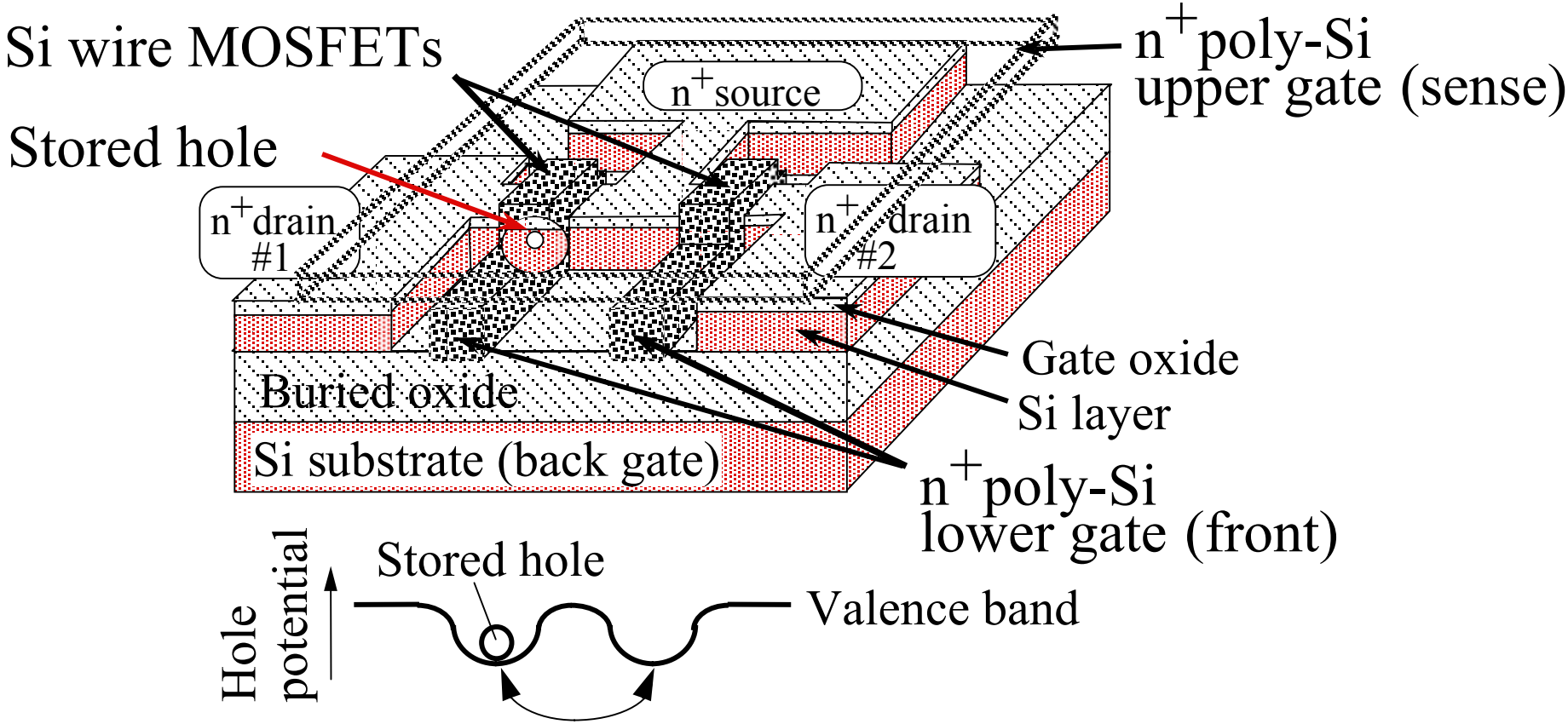


H. Inokawa et al., IEDM, (2001).

New Device for Single-Electron Transfer & Detection (Single-Electron CCD)

Single-Electron CCD

Device Structure

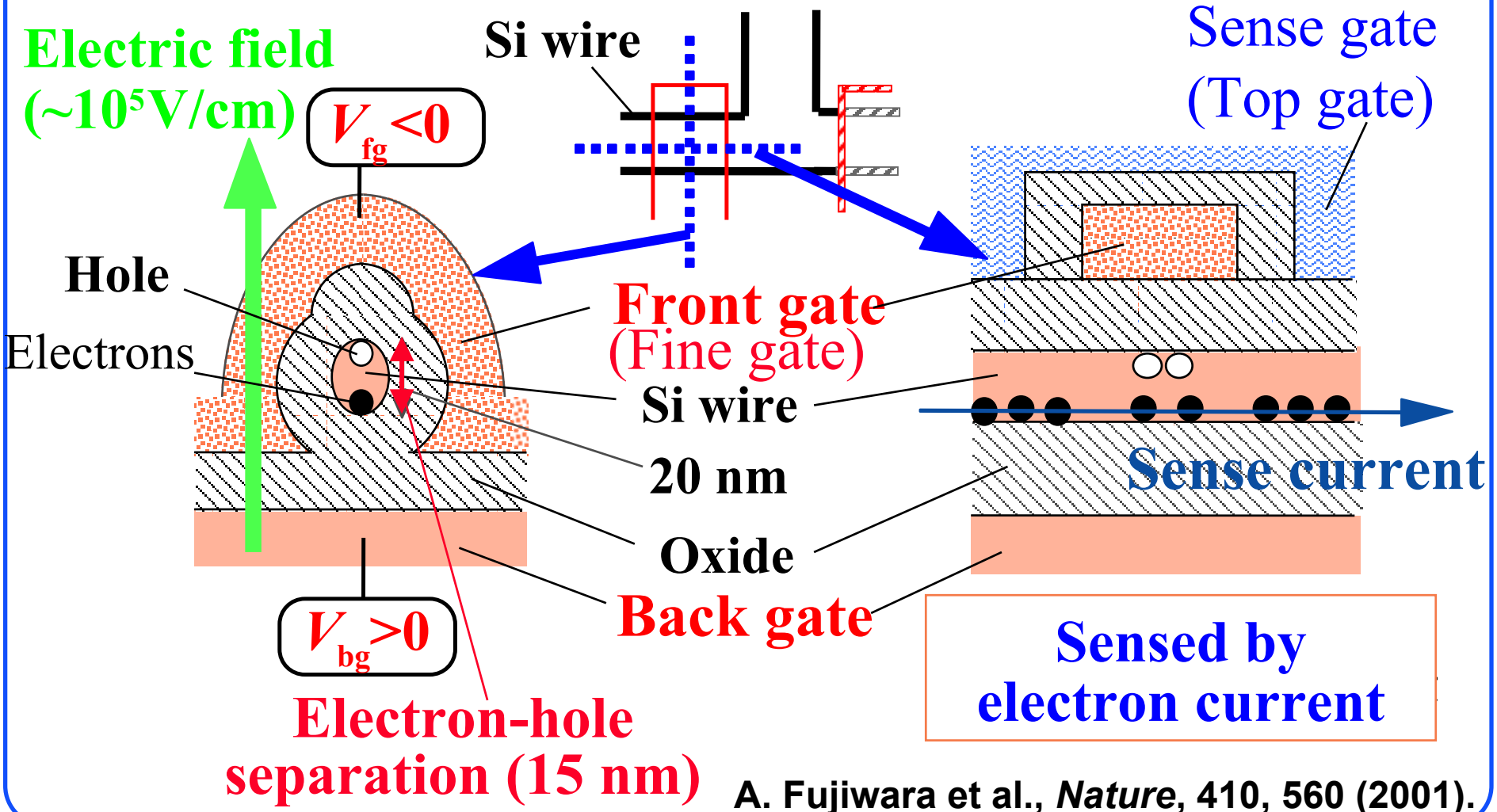


Transfer of single hole

A. Fujiwara et al., *Nature*, 410, 560 (2001).

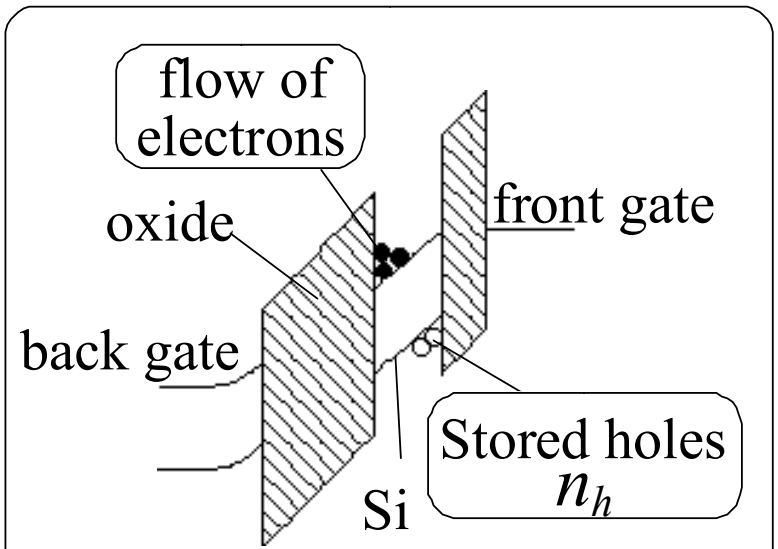
Single-Electron CCD

Structure & Operation principle



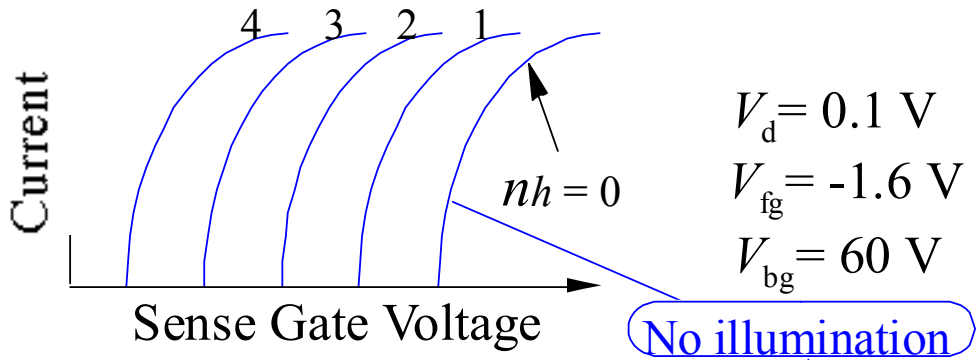
A. Fujiwara et al., *Nature*, 410, 560 (2001).

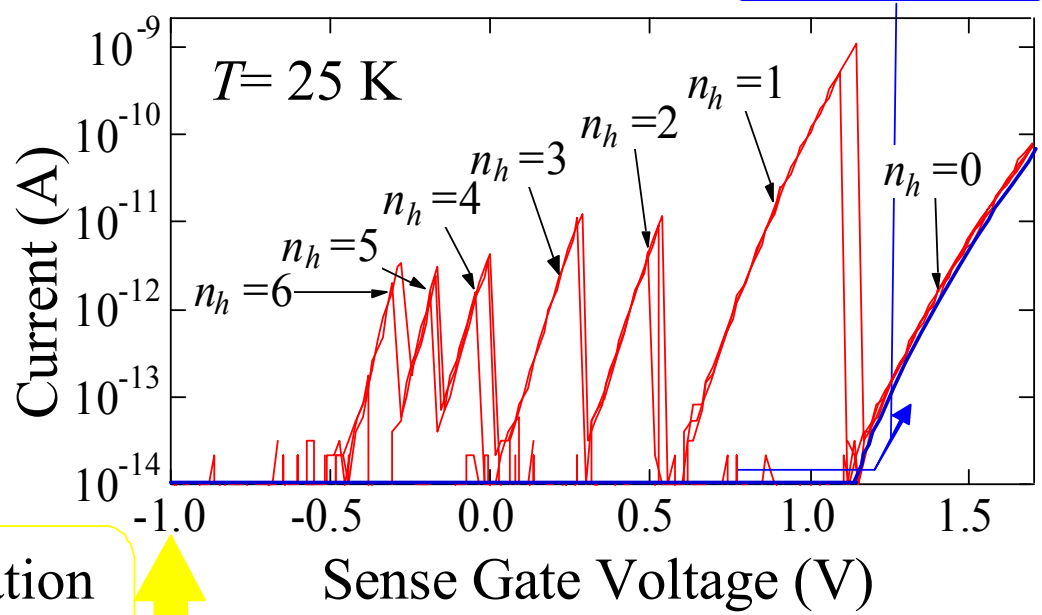
Sensing of Single-Hole



Gate Capacitance ~10 aF
(90 nm-long Si wire MOSFET)

$e^2/C \sim 16$ meV



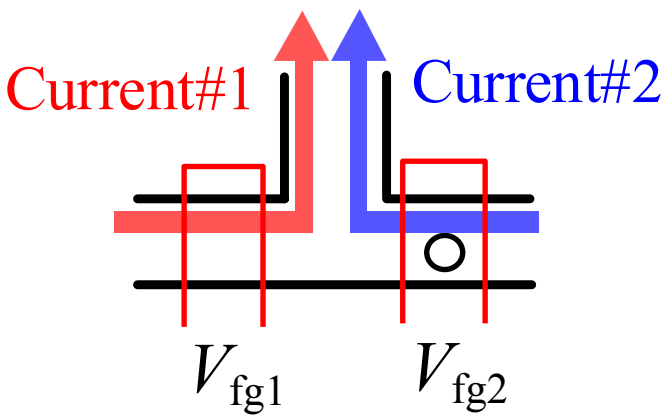


Hole generation by illumination

A. Fujiwara et al., *Nature*, 410, 560 (2001).

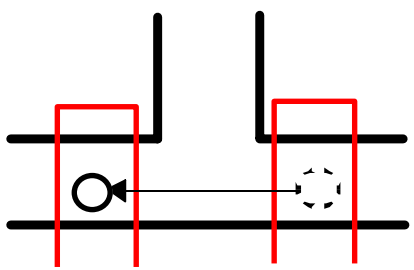
Single-Hole Transfer

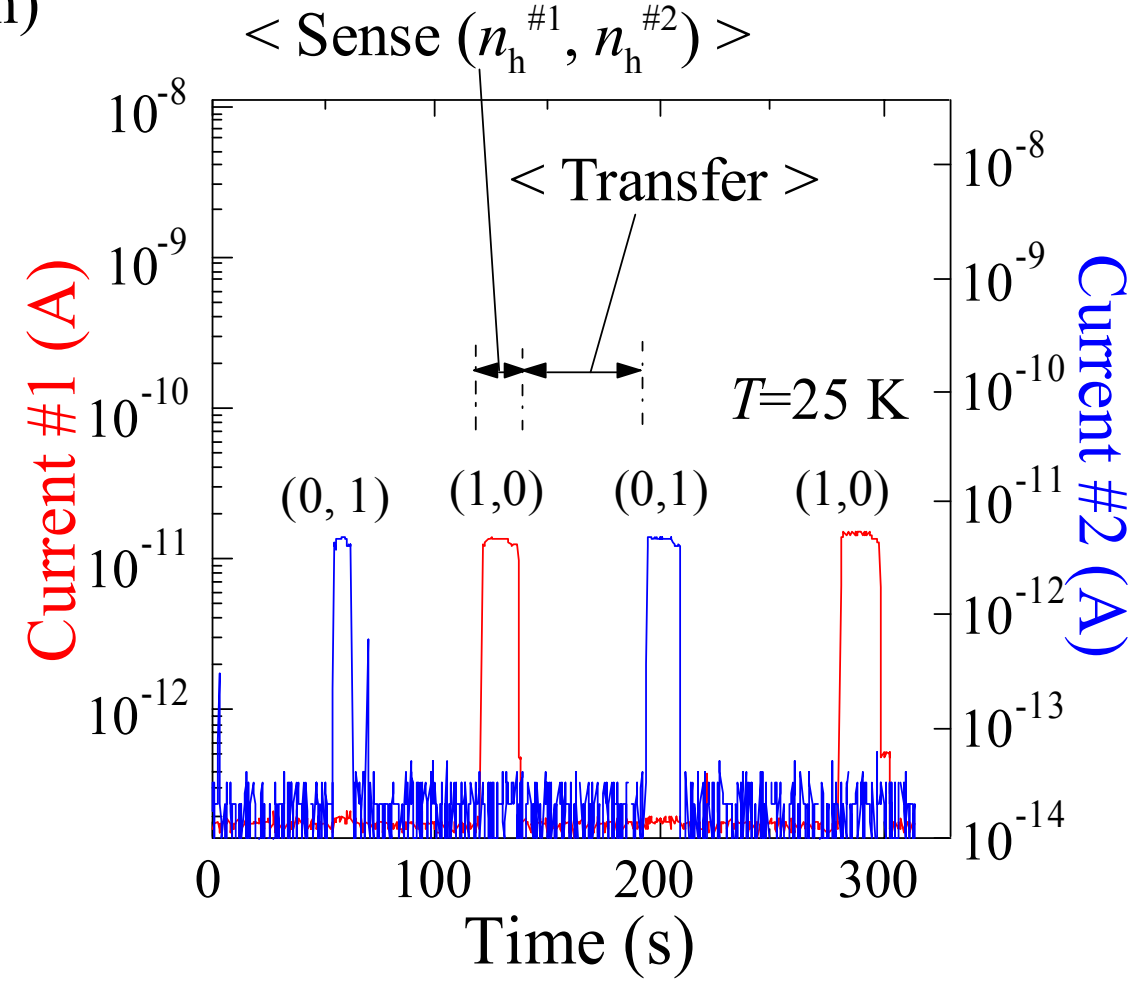
<Sense> V_{sg} =0.88 V (high)



<Transfer> V_{sg} =-1 V (low)

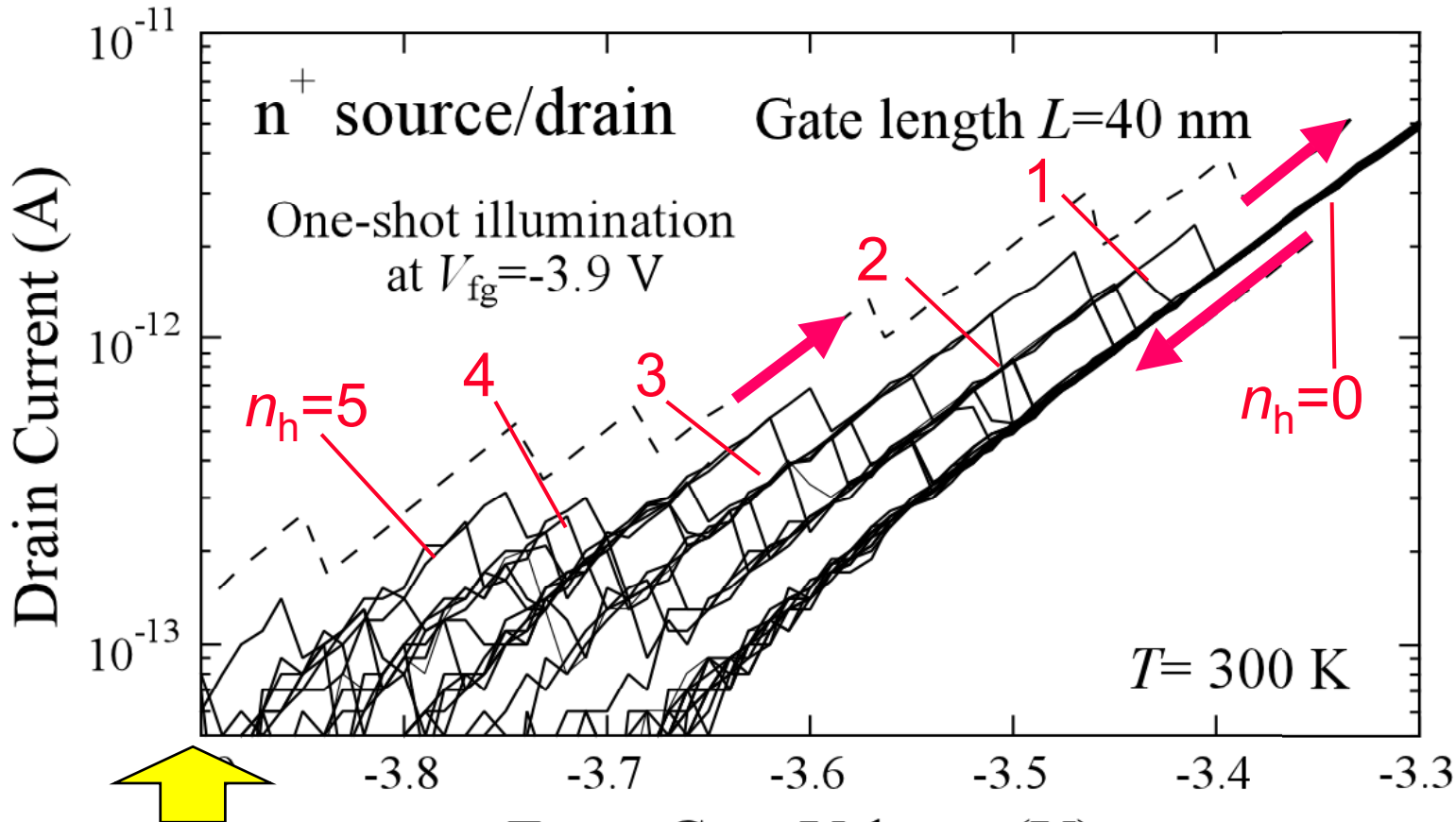
V_{fg1} :-1.3 V ➡ -2.5 V





A. Fujiwara et al., *Nature*, 410, 560 (2001).

Room Temperature Operation of Single-Hole CCD



Hole storage by
One-shot illumination

Summary

PADOX: Pattern-Dependent Oxidation

Self-aligned formation of small Si islands

Small size, Reproducible & Controllable,
Stable operation, Compatible with Si MOS LSI

Multiple-gate structure
Multiple-peak characteristics

Flexible fabrication for SETs

Single-electron Logic Circuit

(Inverter, Adder, X-OR, Multiple-valued logic)

Summary

New Device:
Single-Electron CCD

Simple structures
High temperature operation

Single-electron
Transfer & Ditection

End of Presentation

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